

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

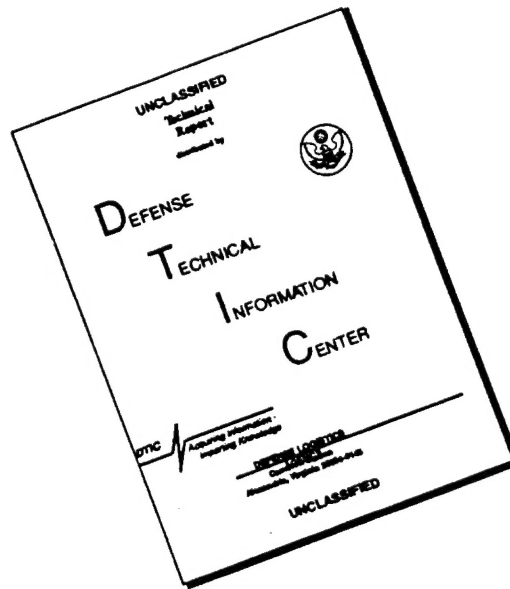
1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED FINAL REPORT - 01 Aug 91 - 31 Jul 96
4. TITLE AND SUBTITLE Two-Dimensional Optical Switching and Logic Arrays for Communication and Computing Systems		5. FUNDING NUMBERS 61102F 2305/DS
6. AUTHOR(S) Professor Cheng		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) EECE Building University of New Mexico Albuquerque, NM 87131		AFOSR-TR-96 0507
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) AFOSR/NE 110 Duncan Avenue Suite B115 Bolling AFB DC 20332-0001		10. SPONSORING/MONITORING AGENCY REPORT NUMBER AFOSR-91-0345
11. SUPPLEMENTARY NOTES 19961017 131		
12a. DISTRIBUTION / AVAILABILITY STATEMENT APPROVED FOR PUBLIC RELEASE: DISTRIBUTION UNLIMITED		DISTRIBUTION CODE

In this final report, we will summarize the broad-ranging research and the many results that we have achieved during this 5-year AFOSR research program. During the past 5 years, we have played a leading role in the development of monolithic optoelectronic integrated circuit (OEIC) technology based on VCSELs. In time these technologies would include heterojunction photo-transistors (HPTs) and photothyristors (PNPNs), PIN and MSM photodiodes, resonance-enhanced photodetectors (REPDs), and heterojunction bipolar transistors (HBTs). We became the first group in the world to demonstrate that the VCSEL's electrical characteristics could be greatly improved by the use of continuous compositional grading by MOCVD. For the first time, we had dropped the operating voltages of VCSELs from 5-10 V down the 2 V, and the series resistance from 200 Ω to less than 50 Ω .

This early impetus allowed us to achieve many different high performance optoelectronic devices based on VCSELs, including several families of optical switches with latching, non-latching, and bistable characteristics (1991), monolithic optical logic gates and logic families (1992), reconfigurable optical routing switches (1993), programmable optical logic gates (1994), high-speed optical transceivers (1995), an optically cascaded multi-stage switching fabric (1995), and a programmable optical logic gate array (1995). Amongst our other contributions to VCSEL technology included the development of high-performance cryogenic VCSELs (77K in 1994; 6K in 1995) and cryogenic optical data links (1996), and the use of chirped multi-quantum wells for a wide operating temperature range (1996).

18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT PAGE 5
--	---	--------------------------------------

DISCLAIMER NOTICE



THIS DOCUMENT IS BEST QUALITY AVAILABLE. THE COPY FURNISHED TO DTIC CONTAINED A SIGNIFICANT NUMBER OF PAGES WHICH DO NOT REPRODUCE LEGIBLY.

CONTRACT AFOSR-91-0345-B

**TWO-DIMENSIONAL OPTICAL SWITCHING AND LOGIC ARRAYS FOR
COMMUNICATION AND COMPUTING SYSTEMS**

Julian Cheng, *Principal Investigator*

THE AIR FORCE OFFICE OF SCIENTIFIC RESEARCH

BOLLING AIR FORCE BASE

DR. ALAN CRAIG, *Program Manager*

ABSTRACT

This program began with the objective of developing a novel two-dimensional optical smart pixel technology that would offer the potential for achieving very-compact, very-high-information-throughput, parallel optical data processing architectures. The technology we had chosen was based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic technologies. We played a leading role in the development of monolithic optoelectronic integrated circuit (OEIC) technology based on VCSELs, including heterojunction photo-transistors (HPTs) and photothyristors (PNPNs), PIN and MSM photodiodes, resonance-enhanced photodetectors, and heterojunction bipolar transistor (HBT) technology. During the course of developing these technologies, we also played a role in advancing the state-of-the-art in VCSEL technology, which was then (in 1991) in a nascent phase of development. Our major contribution to VCSEL technology occurred in 1991, when we became the first group in the world to achieve a significant improvement in the electrical characteristics of VCSELs by the continuous compositional grading of the heterointerfaces using MOCVD growth. This early impetus allowed us to achieve many different high-performance optoelectronic devices based on VCSELs, including several families of optical switches with latching, non-latching, and bistable characteristics (1991), monolithic optical logic gates (1992), reconfigurable optical routing switches (1993), programmable optical logic gates (1994), high-speed optical transceivers (1995), an optically cascaded multi-stage switching fabric (1995), and a cascadable programmable optical logic gate array (1995). Amongst our other contributions to VCSEL technology included the development of high-performance cryogenic VCSELs (1994) and cryogenic optical data links (1995), and the use of chirped multi-quantum wells for a wider temperature range (1996).

At a system level, we had developed several novel optical interconnect architectures as well as a novel approach to smart pixel optical logic. Our most significant achievement here is in proposing and also demonstrating the concept of a dynamically reconfigurable optical switch (1992) for optical networking, long before bus switching became a popular theme in optical interconnects.

FINAL REPORT

FOR

CONTRACT AFOSR-91-0345-B

from

**THE AIR FORCE OFFICE OF SCIENTIFIC RESEARCH
BOLLING AIR FORCE BASE**

DR. ALAN CRAIG, *Program Manager*

on

**TWO-DIMENSIONAL OPTICAL SWITCHING AND LOGIC ARRAYS FOR
COMMUNICATION AND COMPUTING SYSTEMS**

Julian Cheng, *Principal Investigator*

University of New Mexico, Center for High Technology Materials
EECE Building, Room 125, Albuquerque, NM 87131

DATE: September 6, 1996

1. Introduction and a Brief Summary of the Accomplishments of this Program:

In this final report, we will summarize the broad-ranging research and the many results that we have achieved during this 5-year AFOSR research program, which included two no-cost extensions. We had begun this program with the objective of developing a novel two-dimensional optical smart pixel technology that would offer the potential for achieving very-compact, very-high-information-throughput, parallel optical processing architectures. The technology we had chosen was based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic technologies. During the past 5 years, we have played a leading role in the development of monolithic optoelectronic integrated circuit (OEIC) technology based on VCSELs. In time these technologies would include heterojunction photo-transistors (HPTs) and photthyristors (PNPNs), PIN and MSM photodiodes, resonance-enhanced photodetectors (REPDs), and heterojunction bipolar transistors (HBTs). During the course of developing these technologies, we had also played an important role in advancing the state-of-the-art in VCSEL technology, which was then (in 1991) in a nascent phase of development. Our major contribution to VCSEL technology occurred in 1991, when we became the first group in the world to demonstrate that the VCSEL's electrical characteristics could be greatly improved by the use of continuous compositional grading by MOCVD. For the first time, we had dropped the operating voltages of VCSELs from 5-10 V down to 2 V, and the series resistance from 200 Ω to less than 50 Ω . It would be two years before other groups (Sandia in 1993, Honeywell and others in 1994) would achieve these results. This early impetus allowed us to achieve many different high performance optoelectronic devices based on VCSELs, including several families of optical switches with latching, non-latching, and bistable characteristics (1991), monolithic optical logic gates and logic families (1992), reconfigurable optical routing switches (1993), programmable optical logic gates (1994), high-speed optical transceivers (1995), an optically cascaded multi-stage switching fabric (1995), and a programmable optical logic gate array (1995). Amongst our other contributions to VCSEL technology included the development of high-performance cryogenic VCSELs (77K in 1994; 6K in 1995) and cryogenic optical data links (1996), and the use of chirped multi-quantum wells for a wide operating temperature range (1996).

At a system level, we had developed several novel optical interconnect architectures as well as a novel approach to smart pixel optical logic. I think our most significant achievement is in advancing and demonstrating the concept of a dynamically reconfigurable optical interconnect (1992) for optical networking, long before it became a popular theme in optical interconnects.

2. Program Statement: Multi-Functional Smart Pixels:

Smart pixels are defined generically as monolithically integrable, optically interconnected and cascable, multi-functional optoelectronic elements that perform a variety of parallel optical processing functions, including temporal or spatial switching, logic, memory, routing, optoelectronic signal conversion, plus the detection, amplification, and normalization of optical signals. The smart pixel was originally conceived as the optical analog of an electronic processor, replacing many of the electronic functions with optics, and deriving its appeal from the very high interconnectivity and large throughput that optical parallelism provides. However

this has proven to be a technologically difficult challenge, and over the years the relative balance between the optical and electronic functions have shifted, with optics playing a reduced role. At the other end of this spectrum, the smart pixels have become little more than islands of conventional electronic processors concatenated by parallel optical interconnections. This has found expression in emerging commercial optical interconnects such as HP's POLO or Motorola's OPTOBUS, which are passive, parallel, point-to-point interconnects with little additional functionality to leverage their high cost. The objective of this research program is to seek a more meaningful role for optics and the smart pixel that lies somewhere between the all-optical computer and the passive optical link. We wanted to show that optical technologies can perform more complex tasks: turning the passive point-to-point links into dynamically reconfigurable networks, and executing optical logic sequences with a gate-level programmability. Our goal is to develop a monolithic smart pixel technology that take advantage of the very large spatial bandwidth of optics by performing all of the functions mentioned above, and to do so in a reconfigurable manner using a minimum of hardware. This technology has potential applications in high density optical interconnections, high speed optical packet switching networks, and parallel optical data processing.

3. Review of the Technical Approach

Our technical approach is to integrate two-dimensional arrays of emissive and photosensitive devices, as well as electronics, into simple and compact optical /optoelectronic switches that are monolithically integrable, optically cascadable, and multi-functional -- *i.e.*, they are capable of performing a variety of tasks, including optical detection, amplification, switching, logic, memory, routing, and regeneration.. *Functional flexibility is incorporated by making the arrays spatially and functionally reconfigurable, so that they can be programmed to perform many different functions using the same hardware.* Our goal is to construct a simple optical analog of a transistor, which will perform switching and logic functions in a cascadable manner. Each optical switch is a device with both optical and electrical input and output, which provides electronic as well as optical gain.

Figure 1 presents a conceptual picture of a smart pixel-based optical processor system, illustrating some of these required functionalities. Subsumed under these broad functionalities are the parallel optical routing and parallel optical logic functions, which, by introducing the novel element of dynamic reconfigurability, would become the basis for a new reconfigurable optical switching fabric and a programmable optical logic architecture, respectively. We have brought our research on *smart pixels* to a point where the device technologies are sufficiently well-developed to demonstrate some of these important functions of a smart pixel: parallel optical interconnections and complex optical logic.

Two-dimensional integrability offers several important advantages. In addition to the greater density and higher data throughput afforded by an added dimension, it also minimizes chip size as well as the lengths of on-chip electrical interconnections, thereby reducing the overall timing skew and power dissipation per chip compared to those of a large, linear electronic logic gate array, which become very important at high modulation rates. Since successive processor arrays are optically cascadable, the inter-chip optical interconnections provide

electrical isolation between successive stages and minimize interchannel electromagnetic interference. Dynamic reconfigurability, as contrasted to static, allows the network to be programmed rapidly in real time to perform multiple tasks using a minimum of hardware. For example, instead of cascading sequential smart pixel arrays to form a pipeline of distinct processing elements, a programmable optical logic array (OPLA) can simplify and minimize both the optoelectronic and optical hardware.

4. Summary of Technical Achievements during Fiscal Year 1995-1996:

During the final year of this program, our efforts focused on: (1) closing out the first two phases of our previous AFOSR Program, which dealt with the primary optical switches and optical logic gates in the first phase (1991-1994), and with reconfigurable multi-point optical interconnects and programmable optical logic in the second (1994-1996); and (2) transitioning our research to the new continuation AFOSR program, which addresses the extension of reconfigurable switching architectures to an optical networking paradigm through the use of different optical multiplexing technologies. We have already made some progress in this new AFOSR program, which will be discussed in a separate annual report.

As part of the first objective, we focused our work on the following areas: (1) improving optical switching performance by the use of self-aligned HBT technology and new photodetector designs, including the use of resonance enhanced photodetectors (REPDs), (2) characterizing the performance of VCSELs and the optical transceiver/routing switches in high-speed fiberoptic transmission systems, (3) completing the work on cascaded optical logic using a programmable optical logic array, (4) improving the VCSEL's operating temperature range by using chirped multi-quantum-well active regions, (5) reducing the VCSEL threshold and power dissipation by using oxide-confined active regions, and (6) developing efficient low-threshold cryogenic VCSELs.

We summarize the progress that was made:

- (1) Developed an improved self-aligned HBT technology for optical switching applications, achieving a larger bandwidth (4 GHz).
- (2) Fabricated monolithic HBT/VCSEL switches and demonstrated large-signal modulation at 1 Gb/s.
- (3) Characterized the performance of HBT/PIN/VCSEL switches used as an optical transceiver in system transmission experiments across a 1 km optical fiber at 650 Mb/s.
- (4) Demonstrated cascaded optical switching operation of HBT/PIN/VCSEL arrays.
- (5) Demonstrated complex Boolean optical logic operations using optically cascaded arrays of programmable logic gates.
- (6) Demonstrated high performance VCSELs with a wide operating range from 5K to 350K (123°C) and submilliampere threshold current, using nonuniform quantum wells.
- (2) Developed process for selective oxidation and fabricated efficient 850 nm VCSELs with submilliamp currents using oxide-confined active areas.

5. Summary and Review of the Achievements of this AFOSR Research Program

5.a. The Development of VCSEL Technology and VCSEL-Based Optical Data Links

In the early years of this program (1991-93), substantial progress was made in the development of high performance VCSELs. We began with transverse injection, resonant-periodic-gain (RPG) devices (1990), but quickly switched to the development of high-performance, proton-implant isolated VCSELs (1991), which was then hampered by the high dynamic resistance and high operating voltages that resulted from the presence of large energy barriers at the heterojunction interfaces. But using a GRINSCH optical cavity structure and linearly grading the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ composition at all the heterointerfaces in the DBR mirrors, we showed that the problems of a high barrier impedance to carrier transport could be substantially meliorated. In early 1991, we achieved a quantum leap in improving the electrical characteristics of proton-implant-isolated VCSELs, reducing their operating voltages from 5-10 V to <2.5 V and lower their dynamic series resistance from 300Ω to 50Ω . We also demonstrated (1992) an improved operating temperature range (560 K pulsed, and 410K cw) by improving the mode-gain alignment and reducing thermal self-heating, producing more thermally stable electrical characteristics. Further improvements were made (1993) by increasing the doping concentration of the DBR mirrors, which reduced the series resistance to $<20\Omega$ and the *operating* voltages to $<2.0\text{V}$, but at the expense of increased free-carrier absorption and a higher threshold current. In 1994, using a biparabolic grading profile for the hetero-interface, we reduced the barrier heights without the use of higher doping, thereby reducing the operating voltages and the power dissipation, and achieving a high power conversion efficiency (22%) and more thermally stable electrical characteristics. The comparison of the temperature dependence of the electrical characteristics for different doping and grading schemes is shown in figure 1. As seen in Fig. 1(d), the electrical characteristics of these VCSELs changed by very little over a wide temperature range from 80K to 300K, which makes it possible to design simpler laser drive circuits without requiring thermal compensation. Figure 2 shows the lasing and electrical characteristics of VCSELs with bi-parabolic grading. The $16\mu\text{m}$ diameter device has a peak optical output of 15 mW, a low threshold voltage (1.75V), and a power conversion efficiency of 22%, which was then the highest value achieved by any 850 nm GaAs VCSEL.

Current confinement by a selective oxidation process was also developed to achieve VCSELs with low threshold current (1995), mainly for the purpose of reducing the drive current and power dissipation of monolithic switch arrays. The example of an oxide-confined 850 nm VCSEL is shown in figure 3, which has an active area aperture of $4\mu\text{m} \times 3\mu\text{m}$, and shows a submilliampere threshold current, single mode operation, and a moderate optical power output. These devices will be used in the future to produce more power efficient VCSEL and switch arrays.

In 1994, we also demonstrated the first inverted VCSEL structures grown on p-type substrates (figure 4), which provided a configuration that was more conducive to monolithic integration with HBTs, and also allows the use of faster NPN transistor drive circuits for the VCSELs (as used in POLO-2 today).

We also designed optical data links based on VCSELs and studied their transmission characteristics across both single-mode and multi-mode optical fibers at a data rate of > 1 Gb/s. Figure 5a shows the transmission through a 1 km length of single-mode fiber at 650 Mb/s, with a bit-error-rate of $BER < 5 \times 10^{-10}$ (limited by mode-selective loss), while figure 5b demonstrates transmission through a 1 km length of multi-mode fiber at 1 Gb/s, with $BER < 10^{-13}$ was easily achieved. For the single-mode fiber, transmission at 650 Mb/s was achieved, with a $BER < 10^{-13}$.

Our fundamental studies of the temperature dependence of the mode-gain alignment eventually led us to the design of VCSELs that achieved optimum operation at different temperature ranges. In late 1994, we designed the first VCSELs that are optimized for use at cryogenic temperatures from 250K to 6K, and excellent performance was maintained down to temperatures as low as 6K. Power-efficient ($>90\%$ quantum efficiency, 33% wall-plug efficiency, 22 mW peak power, 3 mW dissipation) and high-speed (>12 GHz) VCSEL operation was demonstrated at 77K, representing the best VCSELs ever reported for cryogenic operations (figure 6). To demonstrate their use in high-speed cryogenic optical interconnects (for supercomputers or focal plane array readout), we built a cryogenic optical link and demonstrated > 2 Gb/s large-signal data modulation at temperatures from 77K to 150K, with a bit-error-rate of 10^{-13} and completely temperature insensitive system performance.

3.b. Primary Optical Switches Based on the Integration of VCSELs and HPTs or PNPns

High-performance monolithic optical switches were realized by integrating VCSELs with HPTs and PNPn devices on a single epitaxial structure (1991). By varying the positive feedback between the VCSEL and HPT or PNPn, several families of optical switches with alternatively latching (strong feedback), non-latching (no feedback) and bistable (weak feedback) characteristics (see figure 7) were achieved, with a switching energy of ~ 5 pJ and a switching threshold of 10 nW, 25 μ W, and 100 μ W, respectively. Since a low energy optical input is used to switch on a high power optical source, these switches functionally resemble an optical transistor with high optical gain and contrast. We have also demonstrated single-stage, latching and, non-latching optical logic gates that perform simple, fixed Boolean logic functions: such as AND, OR, INVERT, NAND, NOR, and XOR (figures 8 and 9).

3.C. Dynamically Reconfigurable Optical Routing Switches

Our larger goal was to integrate these elementary switches and logic gates into more complex entities that provide greater functionality, such as two-dimensional arrays that can perform different parallel processing or interconnect functions. The integration must be guided by new optical architectures designed to perform specific functions, such as the routing of formatted optical data, optical combinational logic, or board-to-board optical interconnects, each with different functional requirements. The new optical switch designs and the new architectures based on them must reduce the optical system complexity, which has been anathema to the realization of practical optical processors. To minimize optical beam handling and routing, the smart pixels must be functionally and dynamically reconfigurable, so that they can be programmed rapidly to perform multiple tasks using a minimum of hardware. The fixed function

optical switches and logic gates must give way to a more flexible and reconfigurable optical array architecture in which the functions and signal paths are changed dynamically to perform different functions, while providing a fan-out capability. To achieve this goal we have invented a new reconfigurable binary optical switch design that can perform both spatial routing and optical logic in a programmable manner. Arrays of these switches would form a routing fabric that can spatially reconfigure or re-route the input optical signals to different optical output paths. Complex optical logic functions can be performed using a reconfigurable optical logic architecture in which a single programmable optical logic gate array (POLA) is continuously reconfigured and re-used to perform different tasks from one clock cycle to the next.

Figure 10 shows the multi-functional capability of a binary optical switch array, which can be programmed by simple voltages to perform different optical routing, fan-out, and logic functions. Arrays of these switches can be cascaded to form a multi-stage optical switching network that spatially routes data through parallel optical channels to provide multi-point interconnections between nodes (Fig. 11). These interconnections can also be dynamically reconfigured, thus providing a useful platform for a parallel, spatially-multiplexed optical interconnect switch. Reconfigurable spatial routing of optical data packets was achieved in 1992 using a simple, binary optical bypass-exchange switch consisting of a two-segment HPT each connected to a different VCSEL (figure 12), with each half forming an electrically distinct HPT/VCSEL switch sharing the same optical input port. Programmable spatial routing of the optical input signal to one or more output ports was achieved by setting the appropriate control voltages V_1 or V_2 . The programmable optical spatial routing functions were demonstrated at 20 Mb/s using *binary optical routing switches* integrating two HPT/VCSEL switches in a 1x2 or 2x2 configuration (the latter consisting of two 1x2 switches sharing the same input and output ports). The former provided spatial routing with an optical fan-out of two, while the latter performed optical bypass and exchange operations. Each was strictly an optical switch without any electrical input or output interface.

In 1994, the optical switching speed was increased by an order of magnitude (to ~200 Mb/s) using an improved switch design that also included the ability to carry out optoelectronic signal conversion. In addition to perform switching and to route optical data, each switch node must also be able to communicate with an electronic processor via a simple optoelectronic interface. Therefore, it must be able to perform the optical transceiver functions by converting data interchangeably between the optical and electrical formats.

3.D. A High Speed Optoelectronic Interface: the Integration of VCSELs and HBT Technology

The integration of VCSELs with high speed electronics is driven by the desire to combine the optical source array and its driver circuits into a single technology, and to provide a simple optoelectronic interface for VCSEL-based photonic switching networks. A *dynamically reconfigurable optical interconnect* consisting of arrays of optical routing switches can link many electronic processors together by routing data through parallel optical channels interconnecting individual electronic processors. Each switch provides an optical data link to other nodes, as well as a high speed optoelectronic interface to an associated electronic

processing element. Before the electronic processing elements can communicate with each other through parallel optical channels in the switching fabric, an optoelectronic interface is needed to effect electrical \leftrightarrow optical data conversion, thus performing the optical transceiver functions and allowing the switch to communicate with its electronic control functions.

The VCSEL was monolithically integrated with a GaAs HBT in 1992. This simple optoelectronic switch (figure 13) performed optoelectronic signal conversion and provided a high electrical-to-optical conversion efficiency (up to 150 mW/mA). To incorporate optical switching, a *single-channel*, monolithic three-terminal (3T) HPT/VCSEL switch was used (1993) to combine optical and optoelectronic switching into a single structure, thus providing a *binary optical routing switch* with a simple, high-speed interface to electronics. Electrical inputs can now modulate the switch to produce an optical output, and optical inputs can modulate the switch to produce an electrical output, both of which can be spatially routed. The physical layout, circuit diagram, and the functional configurations of the 3T-HPT/VCSEL switch are shown in figure 13, along with the experimental demonstration of different combinations of electrical and optical switching. The switch can convert an electrical or optical input data packet into an optical or electrical output, and provides a convenient platform for combining electrical and optical data packets into a common format. An optical input P_{in} produces an amplified optical output P_{out} (*optical switching*), while the modulated collector current (or voltage) is sent to an electronic processor as a *switched* electrical signal (*receiver function*). Alternatively, electrical data inputted at the base terminal can modulate the VCSEL to produce a switched optical output (*transmit function*). The first two time traces in figure 13 show the modulated output signal in the presence of *only* the electrical or optical input data, while the last two traces show the modulated electrical and optical outputs when both input data formats are present. The switch performed optical switching at 200 Mb/s, and optoelectronic conversion (*transmit or receive*) at a data rate of >500 Mb/s. Most of the functional capabilities required by a reconfigurable optical routing fabric, including optical switching and optoelectronic signal conversion, have been demonstrated at a data rate of 200 Mb/s, which exceeded the B-ISDN rate of 155 Mb/s. .

3.E. Improved Performance of Heterojunction Bipolar Transistors:

For many potential interconnect functions, the switches must be able to operate at a data rate of ≥ 1 Gb/s. To achieve this, both the VCSEL and the HPT must have sub-nanosecond rise and fall times. The optical switching energy also needs to be reduced to the sub-picojoule level, and a high optical gain is needed for cascaded optical switching operation. Increasing the gain of the HPT while preserving its switching speed requires a trade-off that compromised the switching performance. Our early HPTs achieved a high current gain of up to 600, but its 3 dB bandwidth was limited to ~ 200 MHz. The 3T-HPT switch achieved a bandwidth of 600 MHz, but was limited to a gain of 60. By modifying the HBT design and using a self-aligned technology with lower base resistance, we have improved the unity-gain bandwidth of the HBT to ~ 4 GHz while achieving a sufficiently high current gain (~ 100) for optical switching operations. Using this improved HBT technology, monolithic HBT/VCSEL switching circuits have been realized that can undergo large-signal pseudorandom modulation at a data rate of close to 1 Gb/s, as shown by the wide-open eye diagram in figure 15.

3.F. High-Performance PIN/HBT/VCSEL Switch - Separation of the Photodetection and Gain Functions

In addition to performing the *optical switching, routing, transmit and receive functions*, each switch node must *achieve a sufficiently high optical gain* in order to perform optically cascaded switching operations. This was accomplished (in 1995) by replacing each 3T-HPT by the combination of a HBT and a PIN or MSM photodetector. Separation of the gain (HBT) and photodetection (PIN) functions allowed us to reconcile the conflicting requirements of high current gain, high coupling efficiency, and high speed, which had limited the performance of the 3T-HPT. Using the new PIN/HBT/VCSEL switch design, we achieved a very high differential dc optical gain of 18 and an ac optical gain of 4 per stage, which provided a sufficient power margin to compensate for the systemic optical losses in cascaded, multi-stage switching operation.

The new binary optical/optoelectronic switch (circuit in Fig. 16a, photograph in Fig. 16b) consists of two HBT/PIN/VCSEL switches whose closely-spaced PINs form a single two-segment optical input port. The two switches thus share a common optical input (the PIN pair) and electrical input (base terminal of the HBT). An electrical input modulates either or both HBTs to produce an optical output at either or both VCSELs (*transmit function*). An optical input incident on the PIN pair can likewise modulate either (or both) PIN/HBT/VCSEL switch(es) to produce one or more switched electrical (*receive function*) or optical (*optical switching function*) outputs. By controlling the bias voltages V_{c1} and V_{c2} , the switched signal can be controllably routed to one or more output destinations. Each binary switch node can thus act alternatively as an optical receiver, a transmitter, or an optical routing switch with a fan-out of two. By connecting a linear array of PIN/HBT input nodes to a like number of VCSEL output nodes in a shuffle geometry, a multi-stage optical interconnection network is formed, in which the optical or electrical input signal from any node can be routed optically to any other node through one or more intermediate hops (figure 16c).

Optically-cascaded, multi-stage switching operation has been demonstrated using three linear (1x8) arrays of binary PIN/HBT/VCSEL switches. Figure 16(d) shows the typical dc electrical characteristics of the VCSEL and the PIN/HBT/VCSEL switch, while Fig. 16(e) shows the voltage-current and light-current characteristics of the VCSEL. The first array converts the electrical input data into a modulated optical format P_0 , which then effects optical switching in the second array and produces an amplified optical output P_1 , which in turn optically switches the third array to produce the optical output P_2 . Figure 16(f) shows the differential optical gain of each stage as a function of the input optical power, showing a peak differential dc gain of 18 and cascaded two-stage dc optical gain of 50. Note that the gain would be higher if the thresholds of the two optical switch arrays are more closely aligned.

High-speed modulation of the binary PIN/HBT/VCSEL switch was also demonstrated, as shown in figure 17. Large signal optical switching and optoelectronic data conversion, as well as the spatial routing of the optical data, were achieved at a data rate of close to 500 Mb/s, which is limited by the response of the PIN photodetectors (~700 MHz bandwidth).

The use of the PIN/HBT/VCSEL as an optical transceiver has also been studied. The output of the VCSEL has been coupled into both single-mode and multi-mode optical fibers with a length span varying from 0.5m to 1 km, which is then detected by the PIN segments of another PIN/HBT/VCSEL switch at the receiver end. Optical transmission was successfully demonstrated at a data rate of 650 Mb/ across 1 km span of single-mode fiber, with a bit-error rate of $<10^{-9}$ at an average signal level of -10 dBm. While these simple transceiver circuits may be adequate at a board-to-board interconnect distance of 2 cm, longer length spans will require more optimized receiver designs with lower noise levels.

3.G. Smart Pixels as a Compact Optical Logic Processor: the Programmable Optical Logic Gate Array

Following our earlier demonstrations (1991-1992) of simple Boolean optical logic using latching PNP/VCSEL logic gates and non-latching HPT/VCSEL logic gates, we proceeded to design programmable optical logic gates for a simpler and more functionally flexible optical logic architecture that can perform more complex logic functions using a minimum amount of optical and optoelectronic hardware. Programmable optical logic operations were demonstrated in 1993 using non-latching HPT/VCSEL binary optical switches without an electronic interface. Each array can be programmed at the gate level to perform different logic functions - AND and OR - by setting the threshold of each switch, which logically sums the input signals to produce a switched optical logic output, which can also be spatially routed to different output ports. The binary HPT/VCSEL optical switch was programmed to perform AND or OR logic with variable fan-out at a data rate of ~20 Mb/s, as shown in Fig. 18. In order to execute arbitrary logic sequences, several programmable arrays must be optically cascaded, and a multi-stage optical routing network is needed to reconfigure the optical routing paths between arrays. The complexity of the processor would thus rise exponentially with its functional complexity.

To alleviate this problem, we designed an optical programmable logic gate array (OPLA), whose elements consisted of a monolithic array of binary PIN/HBT input nodes and a monolithic array of VCSEL output nodes, and an optically folded logic architecture that continuously re-uses a single OPLA. (figure 19) The complex logic functions are expressed in the sums of products form using dual-rail logic inputs and the AND and OR logic functions, which are executed by optically cascading sequential logic gate arrays, each of which can be *programmed at the gate level* to perform *different logic operations* (AND or OR) *at selected nodes*, and to *spatially re-route* the optical logic outputs (with *optical gain* and a *selectable fan-out*) to provide the inputs for the next array, from one clock cycle to the next. Since each OPLA is reconfigurable, and the binary routing topology is fixed (shuffle network) from stage to stage, the same array can be re-used during each successive cycle, provided that the logic output of the previous cycle is optically buffered by a latching PNP/VCSEL optical switch array. Thus a single OPLA and optical buffer can constitute the entire logic processor without further hardware, while the programming (control) voltages can be stored electronically as a reduced instruction set.

We have demonstrated programmable optical logic using the improved PIN/HBT/VCSEL switches, which provided a higher optical gain, a higher data rate (~100 Mb/s), and both

electrical and optical logic inputs or outputs. Programmable optical logic was demonstrated using either electrical or optical inputs at 100 Mb/s, and more complex logic functions were achieved by cascading two OPLAs. Figures 20a shows the design of an OPLA containing an array of binary PIN/HBT/VCSEL switch nodes, and 20b shows the experimental arrangement that is used to demonstrate cascaded, multi-stage optical logic operation. An optical (A_{opt}) or electrical (A_{el}) logic input is applied to each input node through the PIN-pair or through the base terminal of the HBT, respectively. This produces amplified currents that modulate the optical output P_{out} of a VCSEL, which is pre-biased below threshold. Depending on the bias and routing control voltages, V_{c1} and V_{c2} , the inputs are spatially routed to one or more VCSEL output ports. The input signals from two different input nodes (e.g., A_{opt} and B_{opt}) can be routed to a single VCSEL output port to be logically summed. Since the VCSEL is a threshold device, these sums can determine the logic outcome, e.g., either (A-OR-B) or (A-AND B) logic operation can be executed, depending on the dc prebias level of each VCSEL. The in-plane pairing of nodes (e.g., shuffle connections) defines the range of possible spatial routing configurations within a single stage, and complete routing of the optical logic signals is accomplished using successive stages, which collectively define a logic operation sequence.

The logic operation of the first OPLA at 100 Mb/s is shown in figures 20c and 20d, using either optical or electrical logic inputs, respectively. The optical logic inputs A and B are applied to the PINs at two different input ports, while the *electrical logic inputs* C and D are applied to the base terminal of each HBT. These inputs produce amplified currents that are routed to and summed at a single VCSEL output port, producing optical logic output (A-OR-B) or (A-AND-B), depending on the VCSEL pre-bias level. The rise and fall times are ~ 5 ns, and the switching energy is ~ 300 fJ.

Figure 21 summarizes the results of a cascaded optical logic sequence, stage-by-stage, starting with the optical logic inputs A and B and electrical inputs C and D. The optical outputs (e.g., A+B and C•D) of the VCSELs in the first logic array provide the inputs for the nodes of the next array. Since each array is programmable at the individual gate level, different cascaded logic operations can be performed in parallel by setting the appropriate control voltages. The optical logic outputs of the first stage - (A+B), (C+D) and (C•D) - are routed to the appropriate nodes in the second array, where they are logically summed. The latter array then performs AND or OR logic on these inputs to produce the optical logic outputs [(A+B)+(C•D)], or [(A+B)•(C•D)], respectively. This demonstration of cascaded optical logic illustrates the flexibility afforded by programmability of the switch arrays. Much greater flexibility can be achieved by replacing the non-latching HPT/VCSEL switches with latching PNP/VCSEL switches. This allows a single programmable logic array to be continuously reconfigured and re-used for each successive logic operation, while an optical buffer memory stores the outputs of the previous stage to provide inputs for the next stage. Arbitrary logic functions can thus be performed using a simple 2-chip architecture. This was not demonstrated, however, because of the lack of resource to mount a serious packaging effort.

6. Students Supported by this Program:

This program supported, in whole or in part, the efforts of several graduate students at UNM, many of whom have graduated. The main contributors to this research effort over the past five years included Ph.D. students Dr. Ping Zhou, Dr. Bo Lu, Dr. Yin-Chen Lu, who have received their Ph. D. degrees, plus Geraldo Ortiz and Drew Alduino, who will soon receive theirs.

7. Impact of this Program:

The technologies developed under this program have had significant industrial interest and support. The continuous compositional grading of the DBR heterointerfaces, which we first demonstrated in 1991, represents an important advance in VCSEL technology, and is in common use today. Hewlett-Packard has had a continuing working relationship with the PI on the monolithic integration of VCSELs with HBT technology, as well as in the optical switching technology. HP has provided very substantial support with equipment grants (~\$230K). The PI has also collaborated with Tektronix in the development of VCSELs for low-temperature operations, and using the technology provided by the PI, faster and more efficient devices have been achieved at cryogenic temperatures for optical interconnect applications. In addition, we have provided custom-designed VCSELs to various companies and universities, including the Air Force Institute of technology, Physical Optics Corp., Optical Concepts Corp. (now Gortex), and HP Laboratories.

8. Publications:

- [1] C. F. Schaus, A. Torres, J. Cheng, C. Hains, Z. Sun, K. Zheng, E. Armour, " Transverse-Junction Vertical-Cavity Surface-Emitting Lasers", *Applied Physics Letters* **58**, 1736, (1991).
- [2] J. Cheng, G. Olbright, R. Bryan, "Binary Arithmetic Using Optical Symbolic Substitution and Integrated Phototransistor- Surface-emitting Laser Logic", *Applied Optics*; Vol. 30, No. 30, pp. 4284-4287, November, 1991.
- [3] J. Cheng, R. P. Bryan, and G. Olbright, "Cascadable Surface-emitting Laser Logic: AND, OR, and XOR", *Electron. Lett.*, **27**, 893 (1991).
- [4] P. Zhou, J. Cheng, C. F. Schaus, S. Z. Sun, K. Zheng, E. Armour, C. Hains, D. R. Myers, G. A. Vawter, "Low Series Resistance High Efficiency GaAs/AlGaAs Vertical-Cavity Surface-Emitting Lasers with Continuously-Graded Mirrors Grown by MOCVD", *IEEE Photonics Technol. Lett.* **3**, 591 (1991).
- [5] J. Cheng, "Parallel Optical Architecture For Binary Arithmetic Using Integrated Arrays of Phototransistor/ Surface-Emitting Laser Logic Gates", *Journal of Optical Computing and Processing*, Vol. **1**, No. 3, pp. 189-197, 1991.
- [6] P. Zhou, J. Cheng, C.F.Schaus, S. Z. Sun, C. Hains, K. Zheng, E. Armour, W. Hsin, D. R. Myers, and G. A. Vawter, "Casacadable, Latching Photonic Switch with High Optical Gain by the Monolithic Integration of a Vertical-Cavity Surface-Emitting Laser and a PNP Photodiode", *IEEE Photonics Technol. Lett.*, Vol. **3**, pp. 1009-1012, November, 1991.
- [7] P. Zhou, J. Cheng, C.F.Schaus, S. Z. Sun, C. Hains, K. Zheng, A. Torres, D. R. Myers, and G. A. Vawter "High-Performance, Latchable Optical Switch and Logic Gates Based on the Integration of Surface-Emitting Lasers and PNP Photodiodes", *Appl. Phys. Lett.* **59**, No. 20, pp. 2504-2506, November 11, 1991.

- [8] P. Zhou, J. Cheng, C.F.Schaus, S. Z. Sun, D. R. Myers, and G. A. Vawter, "Surface-Emitting Laser-Based Bistable Optical Switching Device", *Appl. Phys. Lett.* **59**, No. 21, pp. 2648-2650, Nov. 18, 1991.
- [9] P. Zhou, J. Cheng, C.F.Schaus, S. Z. Sun, D. R. Myers, and G. A. Vawter, "Versatile Bistable Optical Switches and Latching Optical Logic Gates Using Integrated Photothyristors and Surface-Emitting Lasers", 1991 International Electron Device Meeting Technical Digest., pp. 611-614, Dec. 1991.
- [10] P. Zhou, J. Cheng, C.F.Schaus, S. Z. Sun, C. Hains, E. Armour, D. R. Myers, and G. A. Vawter, "Inverting and latching optical logic gates based on the integration of vertical-cavity surface-emitting lasers and photothyristors", *IEEE Photonics Technol. Lett.*, Vol. 4, No. 2, pp. 157-159, Feb. 1992.
- [11] J. Cheng, P. Zhou, C. F. Schaus, D. R. Myers, "Cascadable, high-performance optical switches and optical logic based on vertical-cavity surface-emitting lasers", *SPIE Proceedings on Laser Diode Technology and Applications IV*, Vol. 1634, pp. 488-499, 1992. (Invited Paper).
- [13] J. Cheng, P. Zhou, "Integrable Surface-emitting Laser-Based Optical Switches and Logic Gates for Parallel Digital Optical Computing", *Applied Optics, Special Issue on Optical Computing*, Vol. 31, No. 26, pp. 5592-5603, 1992.
- [14] J. Cheng, P. Zhou, S. Z. Sun, S. Hersee, Y. C. Lu, R. Leibenguth, A. C. Adams, D. R. Myers, J. Zolper, J. Puechner, "Monolithic 2x2 Bypass-Exchange Node for Two-dimensional Optical Interconnection Architectures", *Proc. of the LEOS Summer Topical Meeting on Smart Pixels*, Aug. 1992.
- [15] (Invited) J. Cheng, P. Zhou, S. Z. Sun, and D. R. Myers, "Surface-emitting Laser-based Smart Pixels for Two-dimensional Optical Logic and Reconfigurable Optical Interconnections", *IEEE J. of Quantum Electronics*, Vol. 29, No. 2, pp. 741-756., Special issue on Smart Pixels.
- [16] (Invited) J. Cheng, P. Zhou, "Smart Pixels for Two-Dimensional Arrays", *IEEE Circuits and Devices*, Vol. 9, No. 2, pp. 19-27, March, 1993.
- [17] P. Zhou, J. Cheng, S. Z. Sun, H. Hersee, M. Osinski, J. Zolper, D. R. Myers, and G.A.Vawter, "Surface-Emitting Laser-Based Optical Switching: An Update", *SPIE Vol. 1849, Optoelectronic Interconnects*, pp. 298-306, 1993.
- [18] J. Cheng, P. Zhou, "Optoelectronic Technology for a Reconfigurable Optical Interconnection Architecture", *SPIE Vol. 1850, Laser Diode Technology and Applications V*, pp. 93-99, 1993.
- [19] J. Cheng, P. Zhou, Y. C. Lu, "A Directly-Modulated, Pulse-Compressed, and Time- Multiplexed Source for High-Speed Multiple-Access Networks", *IEEE Photonics Technology Letters*, Vol. 5, No. 8, pp. 905-907, August, 1993.
- [20] P. Zhou, J. Cheng, J. C. Zolper, K. L. Lear, S. A. Chalmers, G.A.Vawter, R.E. Leibenguth, and A.C. Adams, "Monolithic Optoelectronic Switch Based on the Integration of a GaAs/AlGaAs Heterojunction Bipolar Transistor and a GaAs Vertical-Cavity Surface-Emitting Laser", *IEEE Photonics Technology Letters*, Vol. 5, No. 9, pp. 1035-1038, Sept., 1993.
- [21] Bo Lu, Ping Zhou, Y.C.Lu, J. Cheng, R.E. Leibenguth, A. C. Adams, J. L. Zilko, K. L. Lear, J. C. Zolper, S.A. Chalmers, G. A. Vawter, "Monolithic Array of Reconfigurable Binary Optical Switches with Fan-out for Multi-Stage Switching and Interconnection Applications", *Integrated Photonics Research Conference*, pp. 258-259, Feb. 17-19, 1994.
- [22] Bo Lu, Ping Zhou, Y.C.Lu, J. Cheng, R.E. Leibenguth, A. C. Adams, J. L. Zilko, J. C. Zolper, K. L. Lear, S.A. Chalmers, G. A. Vawter, "Reconfigurable Binary Optical Routing Switches with Fan-out Based on the Integration of GaAs/AlGaAs Surface-Emitting Lasers and Heterojunction Phototransistors", *IEEE Photonics Technology Letters*, Vol. 6, No. 2, pp. 222-226, February 1994.
- [23] Bo Lu, Ping Zhou, Y.C.Lu, J. Cheng, R.E. Leibenguth, A. C. Adams, J. L. Zilko, K. L. Lear, J. C. Zolper, S.A. Chalmers, G. A. Vawter, "Binary Optical Switch and Programmable Optical Logic Gate Based on the

Integration of GaAs/AlGaAs Surface-Emitting Lasers and Heterojunction Phototransistors", IEEE Photonics Technology Letters, Vol.6, No. 3, pp. 398-401, March 1994.

- [24] Bo Lu, Ping Zhou, Julian Cheng, K.J.Malloy, "Simulation of the temperature dependence of Vertical-Cavity Surface-Emitting Laser Threshold Current", OELASE 1994, Vol. 2147 on Vertical Cavity Surface Emitting Laser Arrays, pp. 12-21, 1994.
- [25] G. G. Ortiz, Julian Cheng, "High-speed Modulation and Small-signal Circuit Modeling of Deeply-Implanted VCSELs with a GRINSCH Active Layer and Graded Heterointerfaces", SPIE Vol. 2147, Vertical Cavity Surface Emitting Laser Arrays, pp. 28-39, 1994.
- [26] Bo Lu, P. Zhou, J. Cheng, K. J. Malloy, "High Temperature Pulsed and CW Operation and Thermally Stable Threshold Characteristics of Vertical-Cavity Surface-Emitting Lasers Grown by MOCVD", Appl. Phys. Lett., Vol. 65, No. 11, pp. 1337-1339, 1994.
- [27] Julian Cheng, "Monolithic Optical Switching Technology for a Programmable Optical Logic Gate Array", Optics and Laser Technology, Special Issue on Optical Computing, Vol. 26, No. 4, pp.239-249, 1994.
- [28] P. Zhou, B. Lu, J. Cheng, K. Malloy, J. C. Zolper, "Vertical-Cavity Surface-Emitting Lasers with Thermally Stable Electrical Characteristics", J. Appl. Phys., Vol. 77, No. 6, pp.2664-2667, March 1995.
- [29] Y. C. Lu, J. Cheng, P. Zhou, J. Klem, J. C. Zolper, "Modulation Response of Monolithic Integrated GaAs/AlGaAs Optoelectronic Switch for High-Speed Electrical-to-Optical Data Conversion", Electronics Lett., Vol. 31, No. 2, pp. 122-124, March 1995.
- [30] Y. C. Lu, J. Cheng, J. C. Zolper, J. A. Klem, "A Reconfigurable optoelectronic technology for multi-processor networks", Multi-functional Surface-Emitting Laser-Based Integrated Photonic/Optoelectronic Switch for Parallel High-Speed Optical Interconnects", Digest of the OSA Spring Topical Meeting on Photonics in Switching, pp., March 22-24, 1995.
- [31] (Invited) Julian Cheng, Y. C. Lu, Bo Lu, A. Alduino, G. Ortiz, J. C. Zolper, J. Klem, G.A. Vawter, "High speed optical interconnect technology for a reconfigurable multi-processor network", SPIE Proceedings Vol. 2400, Optoelectronic Interconnects III, pp. 160-169, Feb. 1995.
- [32] Y.C. Lu, Julian Cheng, J.C. Zolper, J. Klem, "A reconfigurable optoelectronic interconnect technology for multi-processor networks", Proc. of the 45th IEEE Electronics Component and Technology Conference", pp. 1269-1272, June 1995.
- [33] Y. C. Lu, J. Cheng, P. Zhou, J. C. Zolper, J. A. Klem, "Integrated Optical/Optoelectronic Switch for Parallel Optical Interconnects", Electronics Letters, Vol. 31, No. 7, pp. 579-580, May, 1995.
- [34] Bo Lu, Wen-Lin Luo, C. Hains, J. Cheng, R. P. Schneider, K. L. Lear, S. P. Kilcoyne, and J. C. Zolper, "High Efficiency and High Power Vertical-Cavity Surface-Emitting Lasers Designed for Cryogenic Applications", IEEE Photonics Technology Letters, Vol.7, No. 5, 447-448, May 1995.
- [35] Bo Lu, Y.C. Lu, A. C. Alduino, G. G Ortiz, and Julian Cheng, J. Klem, R. P. Schneider, M. J. Hafich, and J. C. Zolper, "Optically-cascaded, multi-stage operation of a multi-functional binary optical/optoelectronic switch", IEEE Photonics Technol. Lett., Photonics Technol. Lett., Vol. 7, No. 12, pp. 1427-1429, Dec. 1995.
- [36] A. C. Alduino, G.G. Ortiz, C. Hains, Bo Lu, Y.C. Lu, Julian Cheng, R. P. Schneider, J. Klem, and J. C. Zolper, "500 Mb/s operation of a multifunctional binary optical switching fabric", Electronics Letters, Electronics Letters, Vol. 31, No. 18, pp. 1570-1571, Aug. 31, 1995.

- [37] Bo Lu, Y. C. Lu, Julian Cheng, J. A. Klem, M. J. Hafich, J. C. Zolper, "High-Speed, Cascaded Optical Logic Operations Using Programmable Optical Logic Gate Arrays", *Photonics Technology Letters*, Vol. 8, No. 1, pp. 166-168, Jan. 1996.
- [38] G. Goncher, Bo Lu, Wen-Lin Luo, Julian Cheng, S. Hersee, S. Z. Sun, R. P. Schneider, J.C. Zolper, "Cryogenic Operation of AlGaAs/GaAs Vertical-Cavity Surface-Emitting Lasers at Temperatures from 200 K to 6K", *IEEE Photonics Technol. Letters*, Vol. 8, pp. 316-318, 1996.
- [39] (Invited) G.G. Ortiz, A. Alduino, Julian Cheng: "Binary Switching Node Reroutes Optical Signals", *Laser Focus World*, Feb. 1996, pp. 83-89.
- [40] Bo Lu, Y.C. Lu, and Julian Cheng: 'Gigabit-per-sec optical link using optimized low-temperature AlGaAs/GaAs vertical-cavity surface-emitting lasers', *IEEE J. of Quantum Electronics*, Vol. 32, No. 8, pp. 1347-1359, Aug. 1996.

9. Figure Captions:

- Figure 1. The electrical characteristics as a function of temperature, comparing the thermal stability of several VCSEL designs with different interfacial grading profiles and doping levels (as noted in each figure).
- Figure 2. (a) The device structure, and (b) the room-temperature electrical and lasing characteristics, of a high performance 16 μm diameter VCSEL with bipolarobically graded DBR interfaces grown by MOCVD.
- Figure 3. (a) The device structure, and (b) and (c), the room-temperature electrical and lasing characteristics of inverted VCSELs grown on a p-GaAs substrate by MOCVD, with an active area diameter of 16 μm and 24 μm , respectively.
- Figure 4. (a) The room-temperature electrical and lasing characteristics of an oxide-confined VCSEL with an active area of $\sim 4 \mu\text{m} \times 4 \mu\text{m}$. (b) shows the oxidized confinement layers (dark lines), (c) the near-field transverse mode, and (d) top view of the oxidized areas (small rectangle for the confined active area, the larger rectangle for the DBR mirror layers).
- Figure 5. (a) The electrical and lasing characteristics of a proton-implant-isolated 850 nm VCSEL that is optimized for cryogenic operation at 100K. (b) the temperature dependence of its threshold characteristics, (c) the power dissipation as a function of temperature and optical output, and (d) their high-speed data modulation characteristics at up to 1 Gb/s.
- Figure 6. The optical transmission characteristics of a 950 nm VCSEL-based optical link across (a) a 1 km length of single-mode fiber at a data rate of 650 Mb/s, and (b) a 1 km length of multi-mode fiber at a data rate of 1 Gb/s.
- Figure 7. The epitaxial structures and optical switching characteristics of three types of monolithic optical switches based on the integration of a VCSEL and a heterojunction

phototransistor or photothyristor. Latching, non-latching, or bistable switching characteristics were achieved by varying the strength of the positive optical feedback within each device.

Figure 8. (a) The latching switching characteristics of a PNP/VCSEL switch, and the demonstration of (b) logic-AND and, (c) logic-OR operation using latching optical logic gates.

Figure 9. The epitaxial structure of a monolithic PNP/VCSEL-based INVERTING logic gate, and the demonstration of latching logic-NOR (a) and logic-NAND (b) operation.

Figure 10. The functions of a programmable and optically-cascadable binary optic switch array consisting of segmented optical input ports and VCSEL optical output ports, which can perform optical switching, routing, logic, and fan-out in a dynamically reconfigurable fashion. These multi-functional switch arrays can be optically cascaded to perform sequential optical logic or multi-stage optical routing operations.

Figure 11. An optically-cascaded, multi-stage switching network using arrays of reconfigurable binary routing switches whose nodes perform the optical transceiver or spatial routing functions. Many nodes can communicate with other nodes simultaneously through parallel optical paths in the switching fabric, which can be dynamically reconfigured.

Figure 12. The design (circuit layout and photomicrograph), the epilayer and device structure, and the experimental demonstration of the optical bypass-exchange routing operations of a monolithic, reconfigurable, binary optical routing switch with (a) 2x2 and (b) 1x2 configuration.

Figure 13. (a) Photomicrograph, and (b) circuit diagram and the input/output functions, and (c) epilayer structure and device layout, of a monolithic 3T-HPT/VCSEL switch. (d) The experimental switching data, with traces 1 and 2 showing the electrical output E_{out} , represented by the amplified collector current I_c , in the presence of either the electrical input data E_{in} or the optical input data P_{in} , respectively. Traces 3 and 4 show the electrical output E_{out} and the optical output P_{out} , respectively, when both P_{in} and E_{in} are present. (e) Eye diagrams at 200 Mb/s, showing the conversion of optical and electrical input data into optical and electrical outputs.

Figure 14. (a) The lay-out, circuit design, and epilayer structure of a monolithic HBT/VCSEL switch. (b) Its dc characteristics and electrical-to-optical conversion efficiency.

Figure 15. (a) The layout of a monolithic HBT/VCSEL switch with a self-aligned HBT design, (b) the differential current gain of the HBT as a function of current density, (c) typical common-emitter characteristics, and (d) the small-signal modulation response of the switch, showing a bandwidth of 4.2 GHz.

Figure 16. (a) The circuit design and (b) device layout of a reconfigurable binary PIN/HBT/VCSEL routing switch, and (c) optically cascaded switching operation using these switch arrays. (d) The common-emitter characteristics of the HBT, with a

current gain of ~ 140 , (e) the electrical and lasing characteristics of the VCSEL ($16\ \mu\text{m}$ diameter), whose slope efficiency is 36%, and (f) the differential dc optical gain of each of two switch stages under optically-cascaded switching operation, with a maximum gain of 18 per stage.

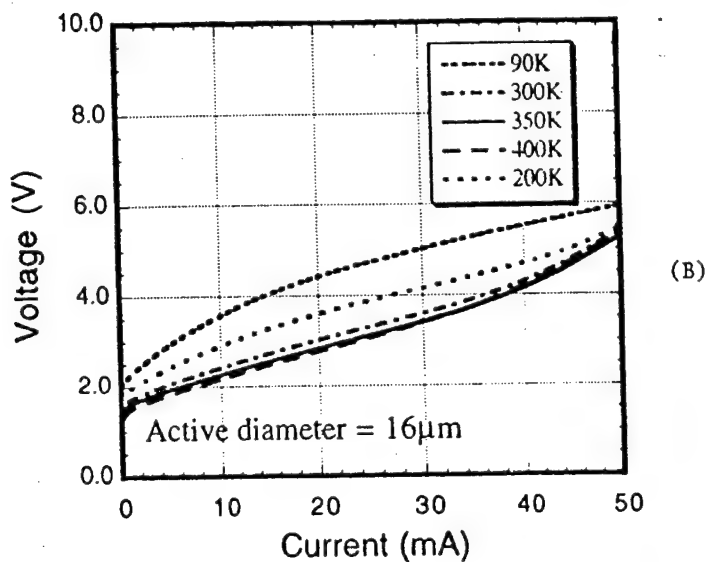
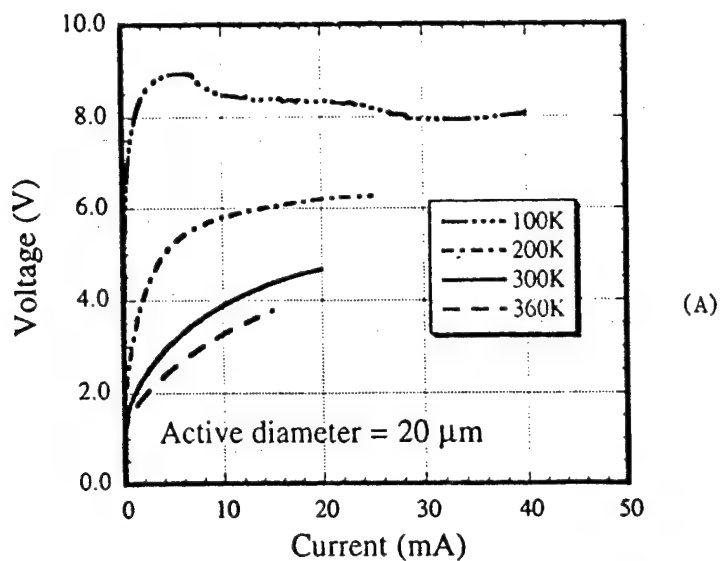
Figure 17. (a) The circuit design, (b) epilayer structure, and (c) photomicrograph of an improved reconfigurable binary PIN/HBT/VCSEL optical routing switch, (d) its electrical-to-optical switching characteristics, (e) its optical switching characteristics, and (f) its optical routing functions, at a data rate of $\sim 500\ \text{Mb/s}$.

Figure 18. Demonstration of programmable optical logic (AND and OR) using a binary optical routing switch.

Figure 19. A schematic representation of the design of a programmable optical logic gate array consisting of integrated arrays of optically cascaded binary PIN/HBT/VCSEL switches, whose functions (logic, routing, fanout) can be programmed at the individual gate level. A logic processing sequence can be executed with an optically-folded architecture, using only a single programmable logic gate array that is reconfigured and re-used from one cycle to the next, while the optical outputs of the previous cycle are stored in a latching optical buffer memory.

Figure 20. (a) The circuit design of a programmable logic gate (inset), and the experimental arrangement used to demonstrate optically cascaded logic operation using two programmable optical gate arrays. Optical logic functions - AND and OR - are performed using (a) optical, and (b) electrical logic inputs and a programmable optical logic gate array. The maximum data rate here is $100\ \text{Mb/s}$.

Figure 21. Two-stage, cascaded optical logic functions on four logic inputs - electrical inputs A and B, and optical inputs C and D. The first stage produces logic outputs: (a) $(A+B)$ and $(C \cdot D)$, and (b) $(A+B)$ and $(C+D)$. The second stage operates on the logic outputs of the first stage, fans-out the logic signals, and performs the logic functions - OR and AND - on these cascaded logic inputs.



JULIAN CHENG
UNIV. OF NEW MEXICO

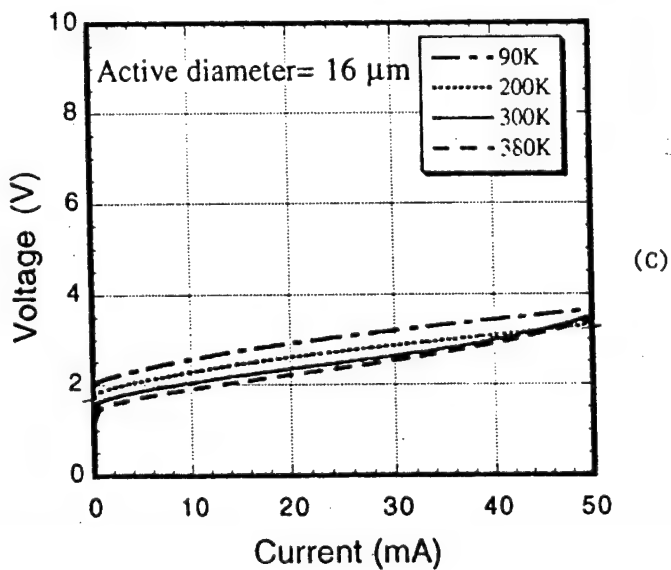


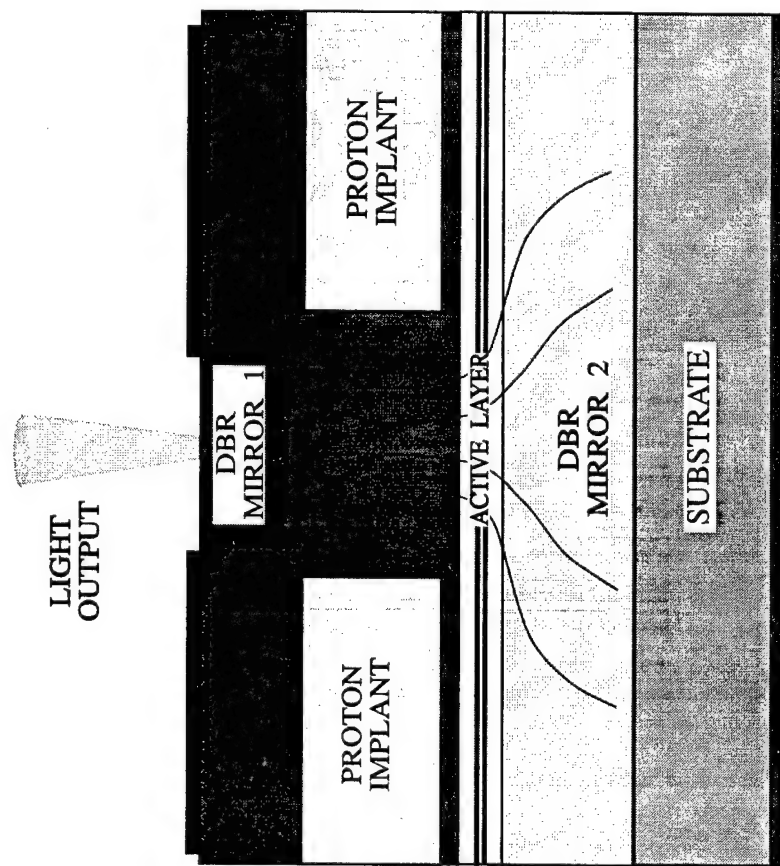
FIGURE 1 .



UNIVERSITY OF NEW MEXICO CENTER FOR HIGH TECHNOLOGY MATERIALS

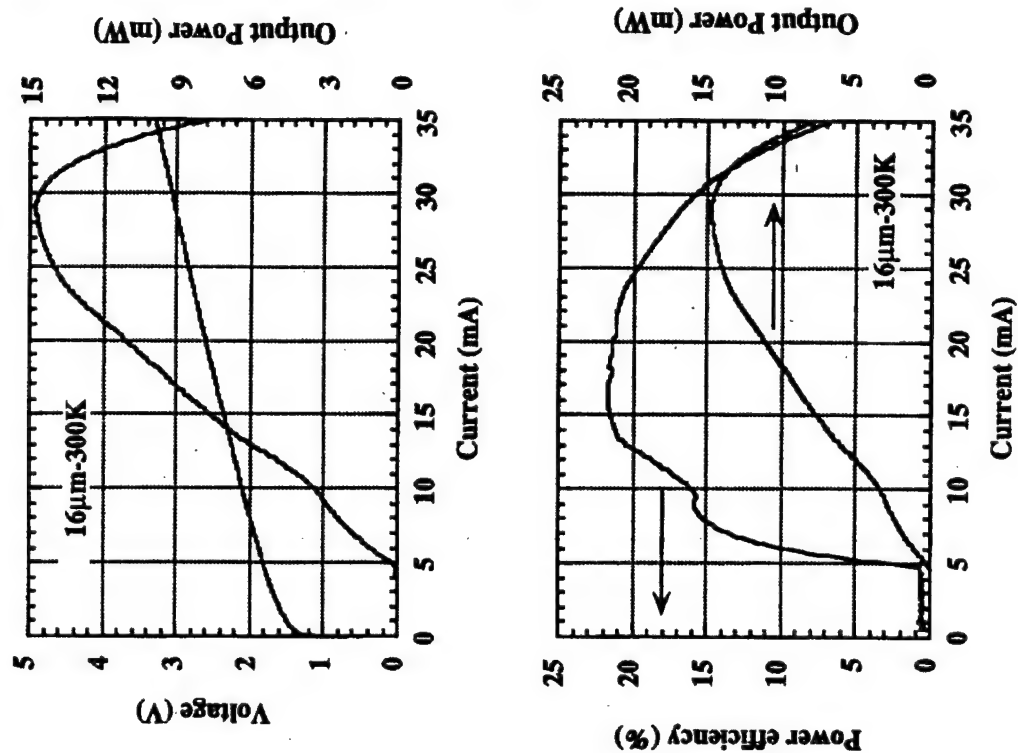
JULIAN CHENG

PROTON-IMPLANT-ISOLATED VCSEL



(a)

FIGURE 2.

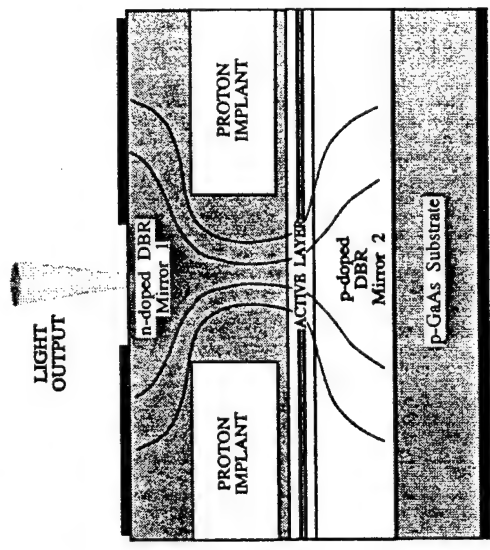


(b)

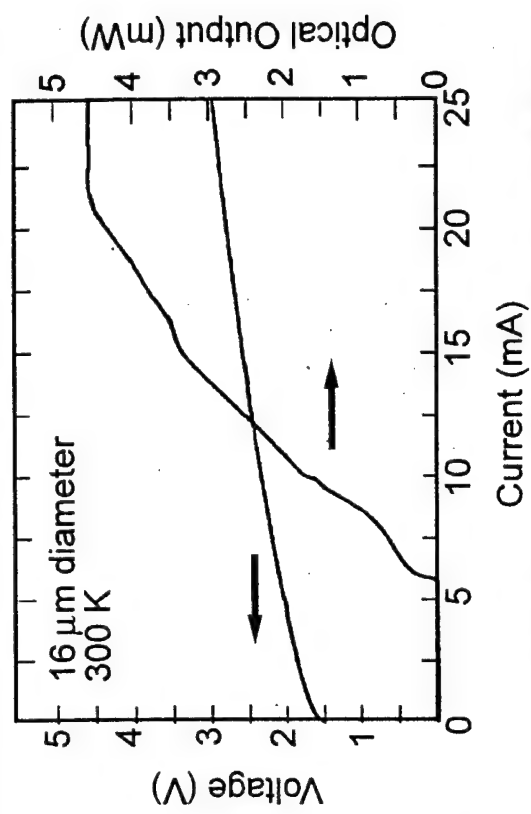
CHARACTERISTICS OF GaAs VERTICAL-CAVITY SURFACE-EMITTING LASER GROWN ON P-TYPE SUBSTRATES

Julian Cheng, University of New Mexico, Center for High Technology Materials

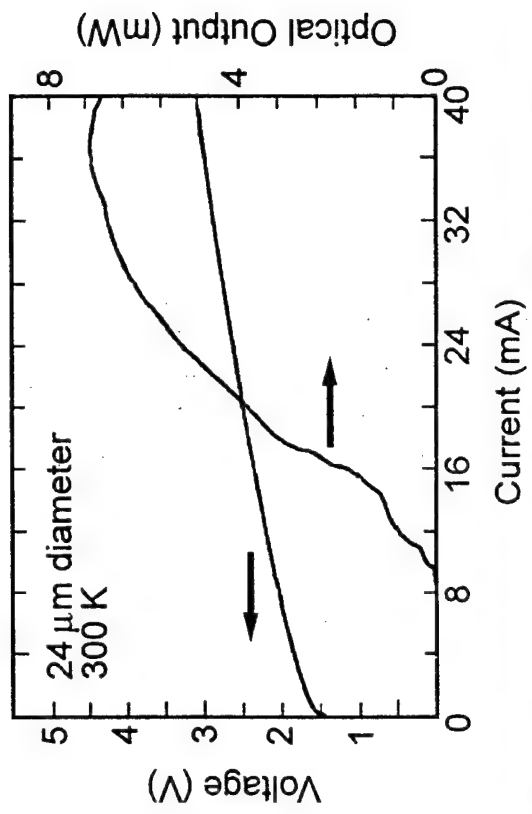
PROTON-IMPLANT-ISOLATED VCSEL



(a)



(b)

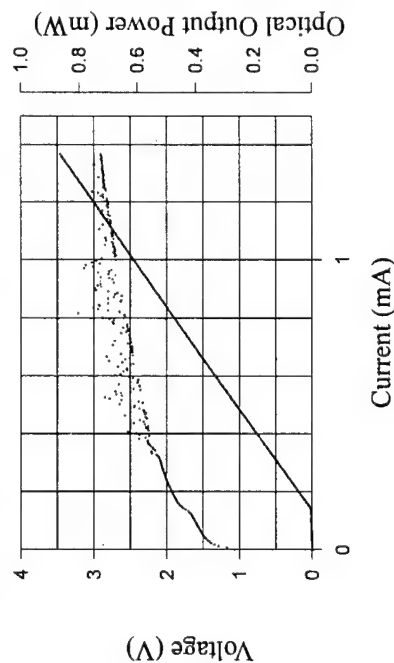


(c)

FIGURE 3.

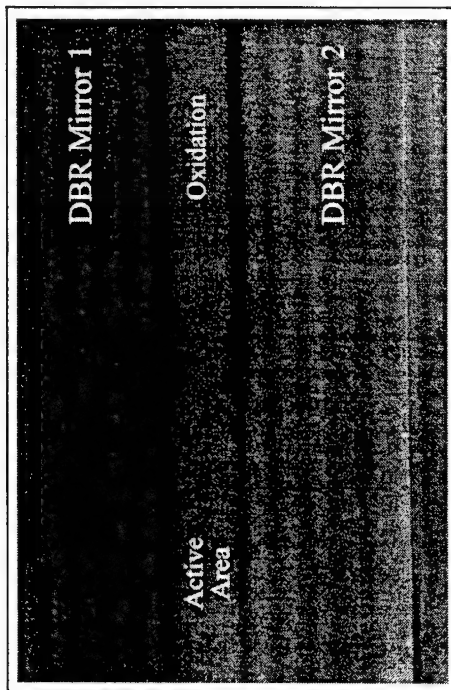
LOW-THRESHOLD OXIDE-CONFINED VERTICAL-CAVITY SURFACE-EMITTING LASER

Lasing Characteristics of Oxide-Confining VCSEL



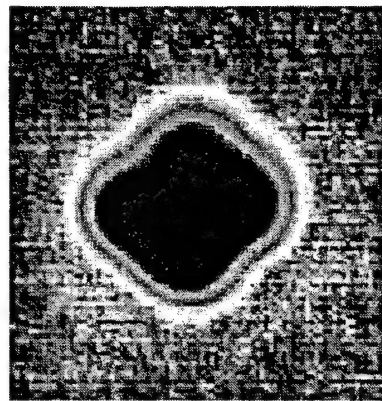
(a)

SEM Cross-Section of Oxidized VCSEL



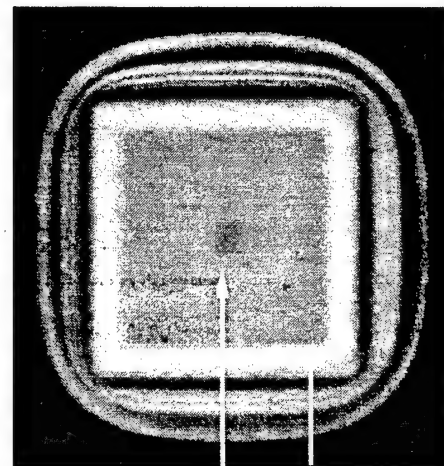
(c)

Single Transverse Mode
VCSEL



(b)

Oxidized VCSEL



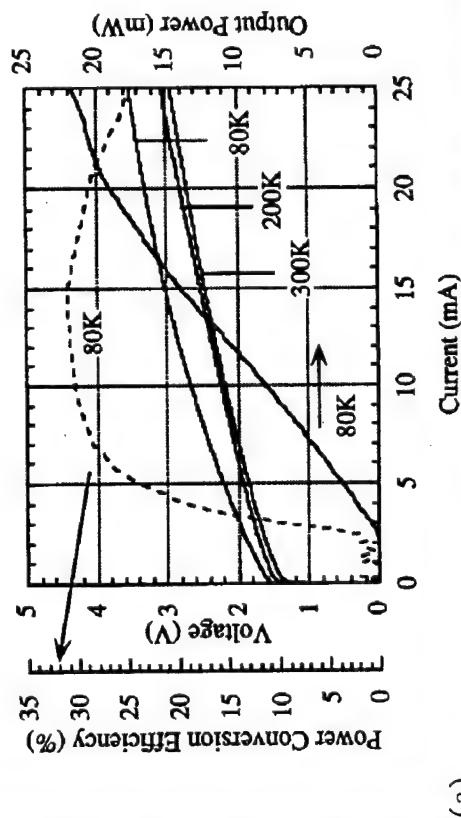
(d)

FIGURE 4.

EFFICIENT CRYOGENIC VERTICAL-CAVITY SURFACE-EMITTING LASERS FOR OPTICAL READ-OUT OF FOCAL PLANE ARRAY DATA

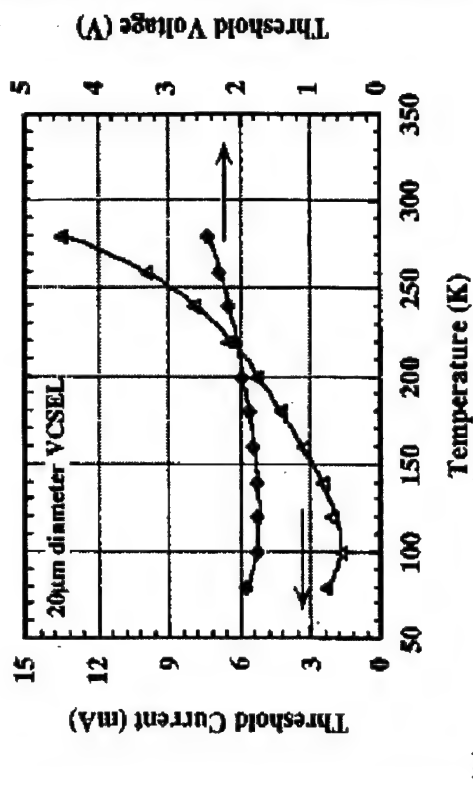
Jiuhua Cheng, University of New Mexico, Center for High Technology Materials

VCSEL Optimized for 100K Operation



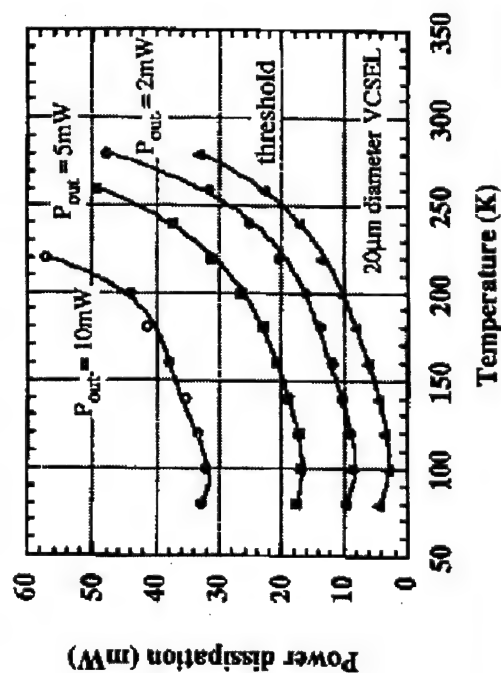
(a)

THRESHOLD CURRENT AND VOLTAGE



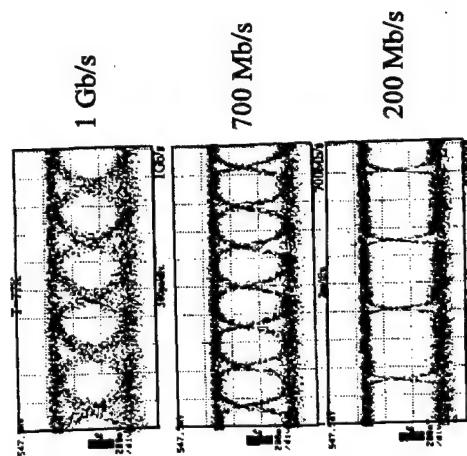
(b)

ELECTRICAL POWER DISSIPATION AS A FUNCTION OF OPTICAL OUTPUT



(c)

ELECTRICAL MODULATION OF VCSEL AT 77K



(d)

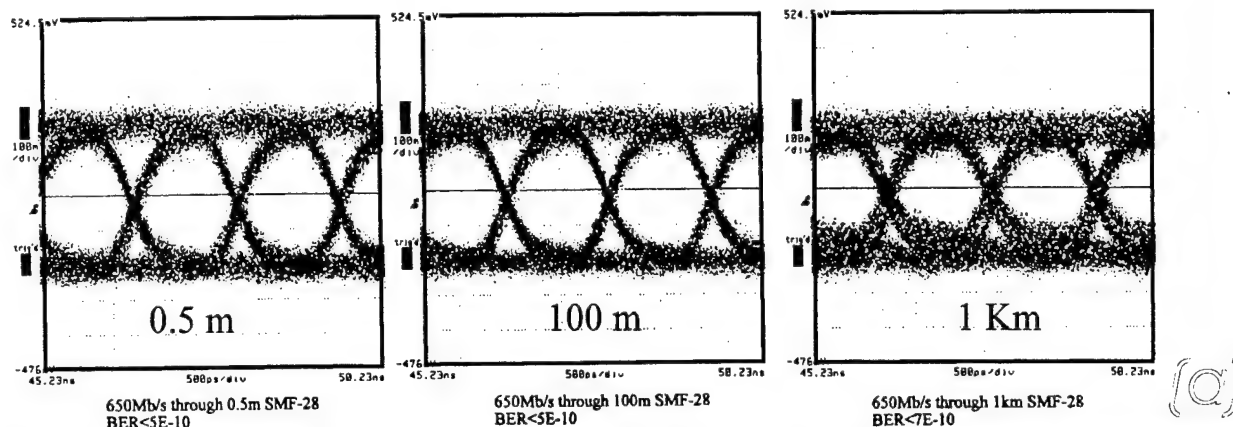
FIGURE 5.



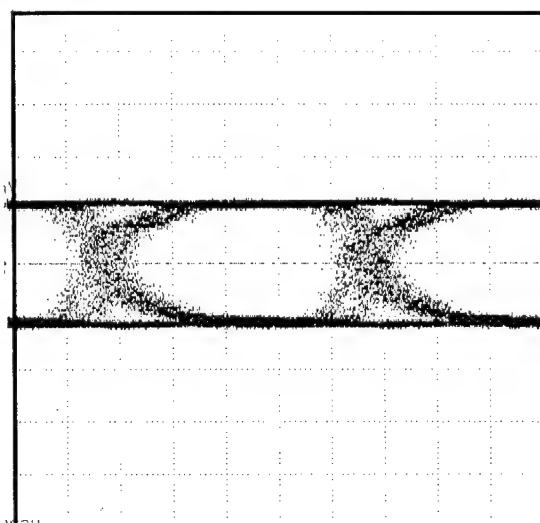
CENTER FOR HIGH TECHNOLOGY MATERIALS
UNIVERSITY OF NEW MEXICO

JULIAN CHENG

650 MB/S TRANSMISSION OF 850 NM VCSEL THROUGH A SINGLE-MODE FIBER



1 Gb/s, $(2^{23}-1)$ NRZ, PRBS Data Transmission through 1km of Multi-Mode Fiber



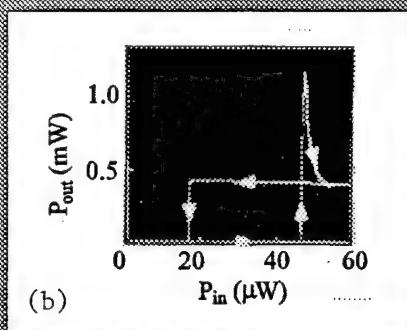
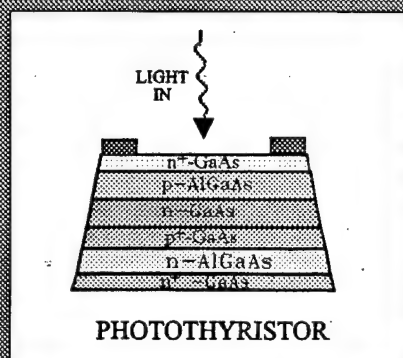
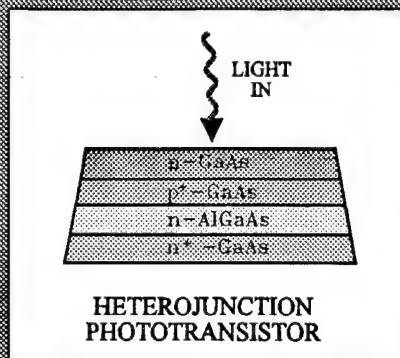
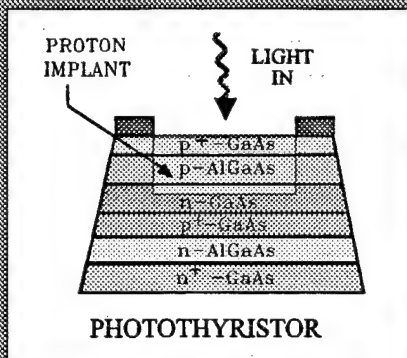
200 ps/div.

$I_{bias}=8.19$ mA
DATA=400 mV
 $I_{pd}=63.3$ uA

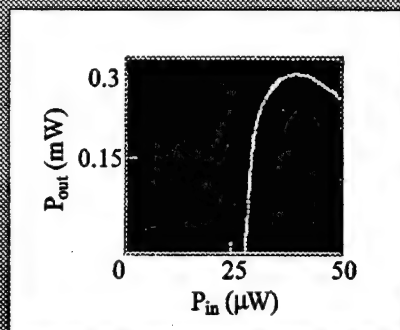
Bit Error Rate < 1E-13

(b)

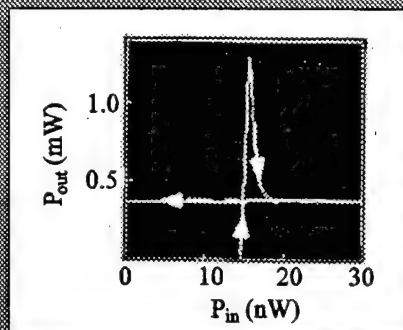
FIGURE 6.



OPTICALLY BISTABLE
PNP/VCSL SWITCH



NON-LATCHING
HPT/VCSL SWITCH



LATCHING
PNP/VCSL SWITCH

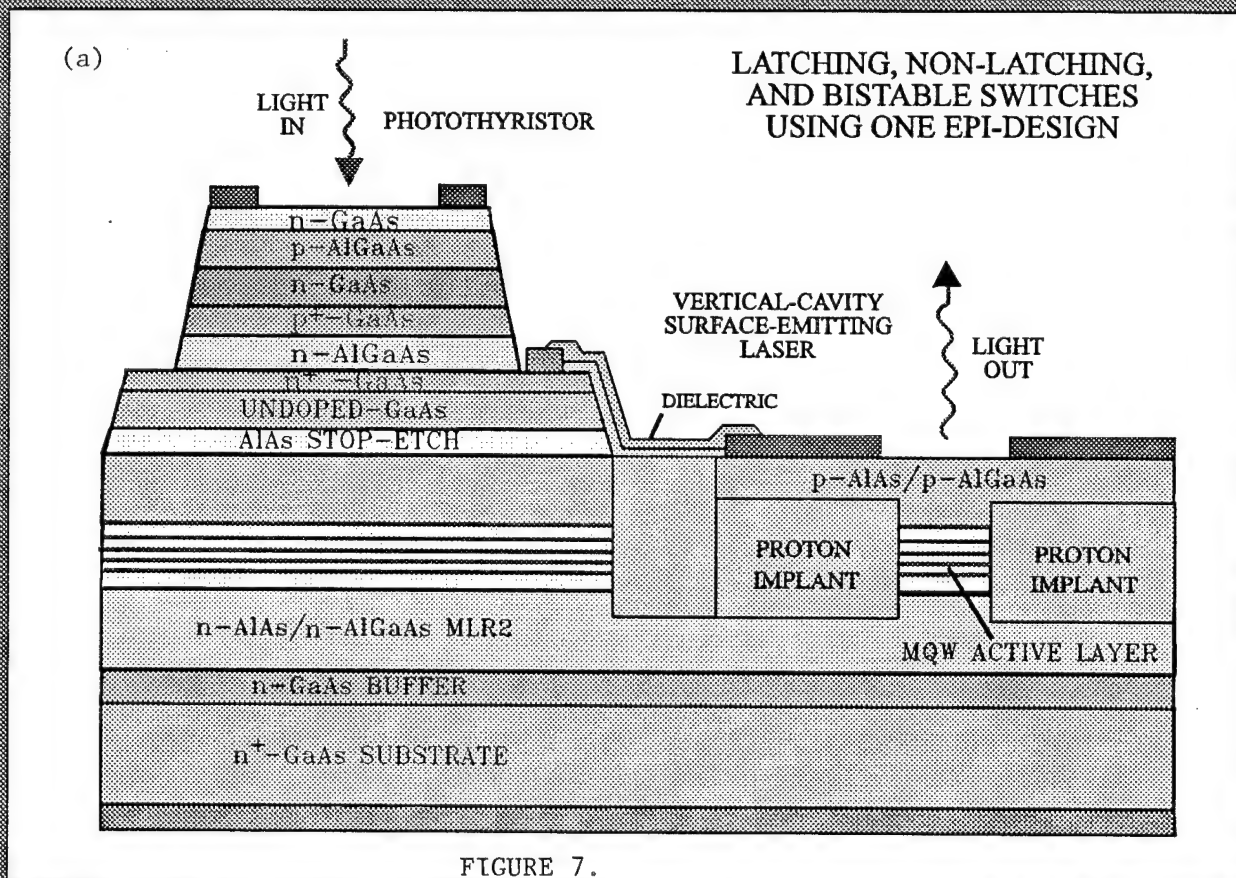
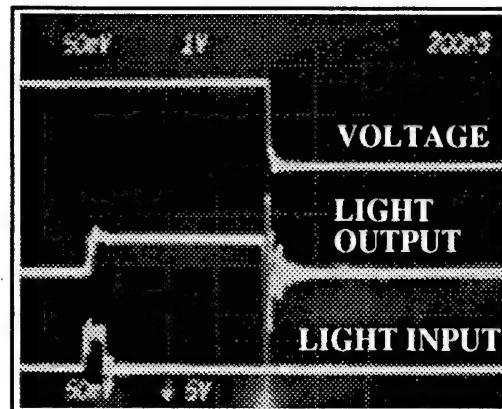


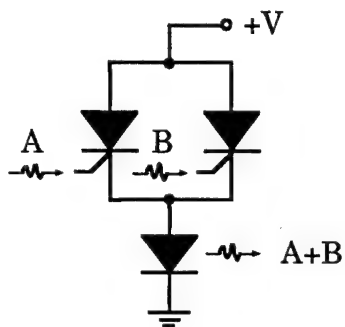
FIGURE 7.

LATCHING VCSEL/PNPN OPTICAL SWITCH

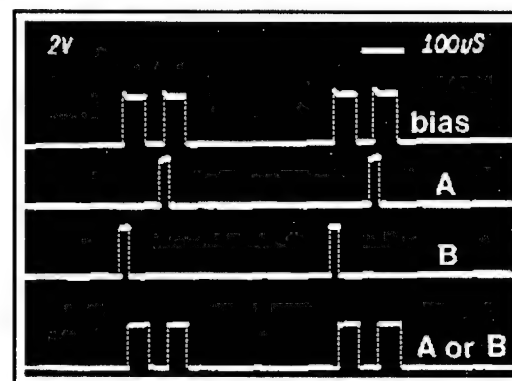
(a)



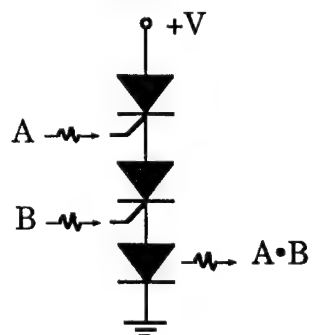
OR



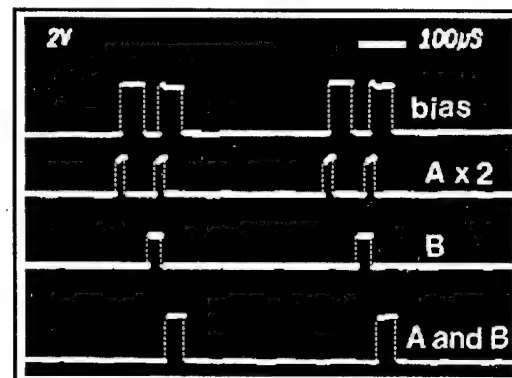
(b)



AND

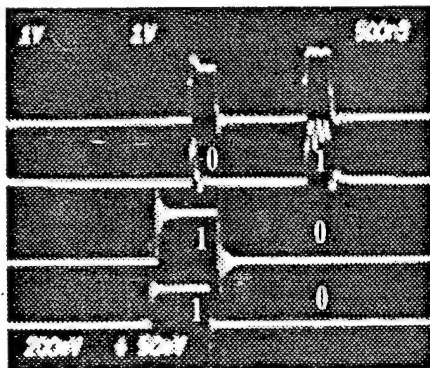
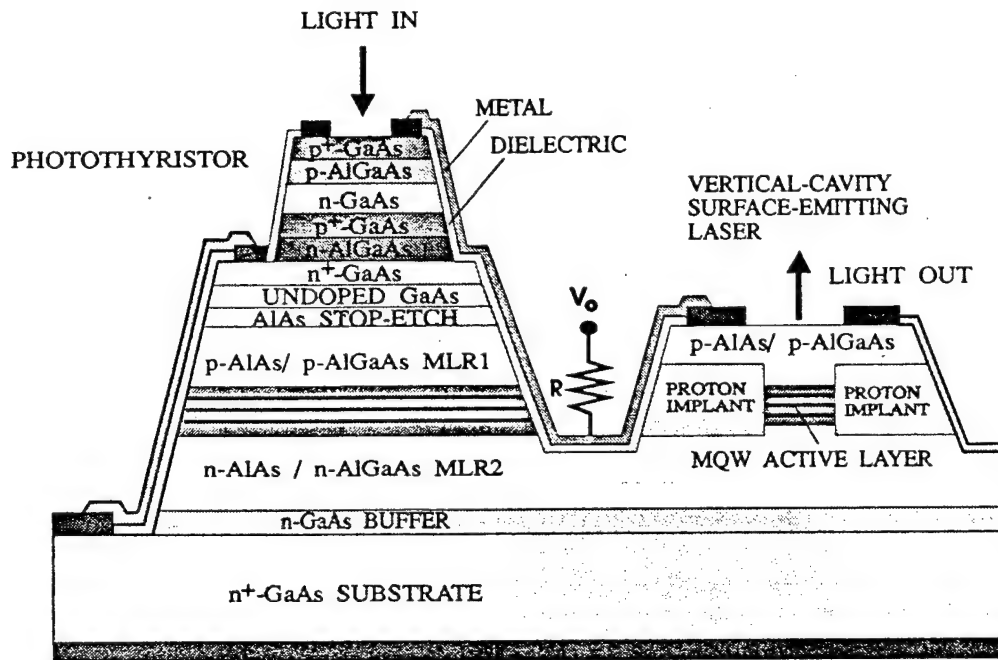


(c)

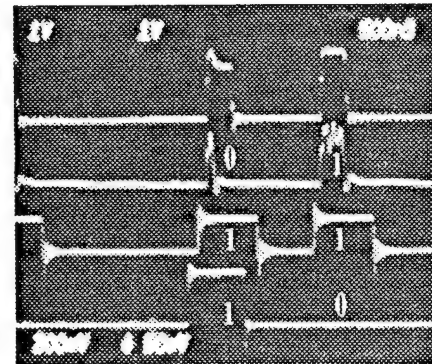


J. CHENG/ UNM-CHTM

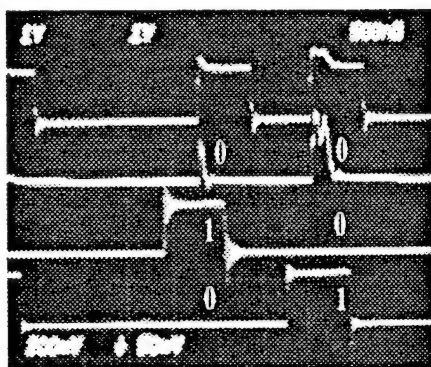
FIGURE 8.



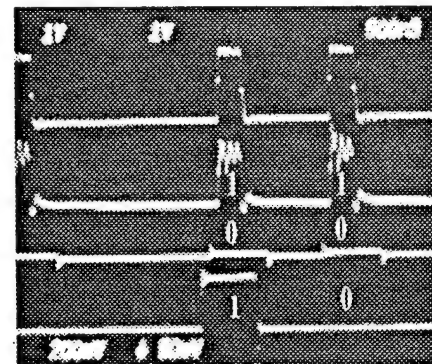
BIAS
VOLTAGE
OUTPUT
INPUT I
INPUT II



BIAS
VOLTAGE
OUTPUT
INPUT I
INPUT II



BIAS
VOLTAGE
OUTPUT
INPUT I
INPUT II



BIAS
VOLTAGE
OUTPUT
INPUT I
INPUT II

(a) OPTICAL NOR GATE

(b) OPTICAL NAND GATE

FIGURE 9.

PROGRAMMABLE OPTICAL SWITCH ARRAY FUNCTIONS

JULIAN CHENG

UNIVERSITY OF NEW MEXICO, CENTER FOR HIGH TECHNOLOGY MATERIALS

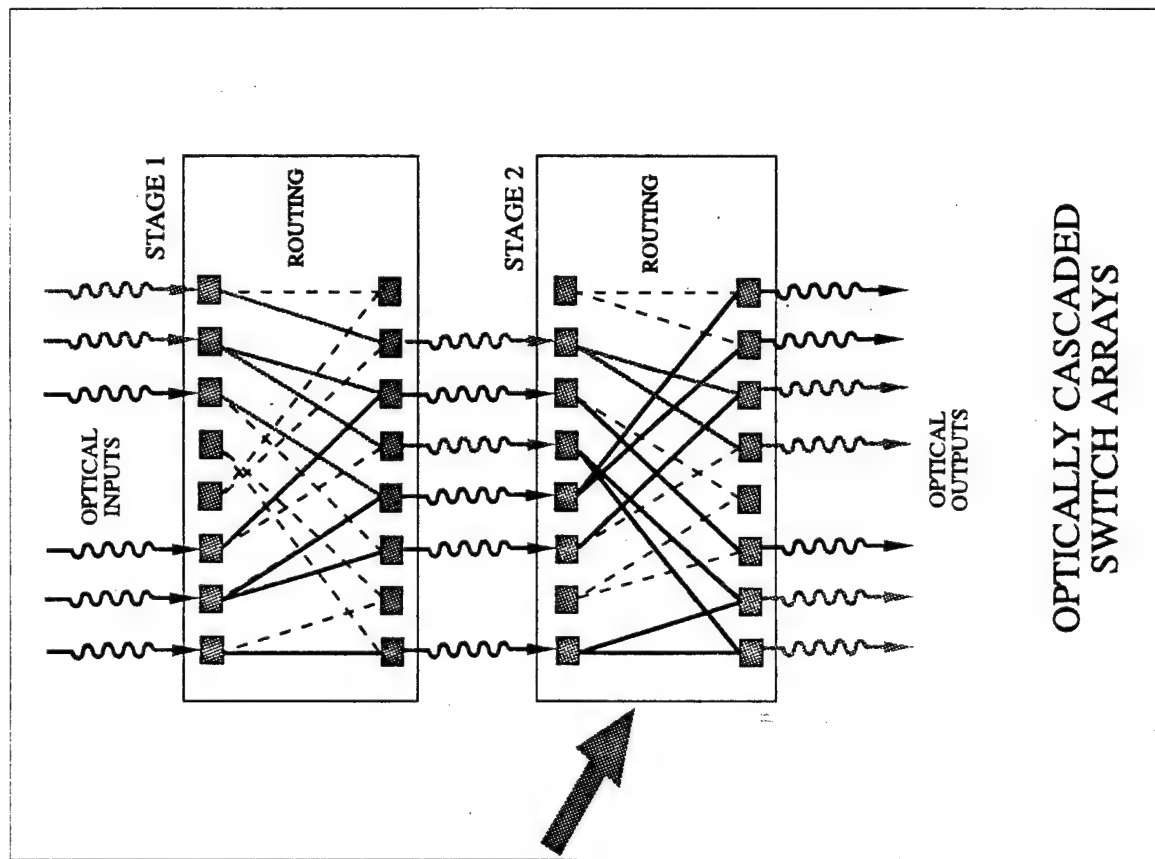
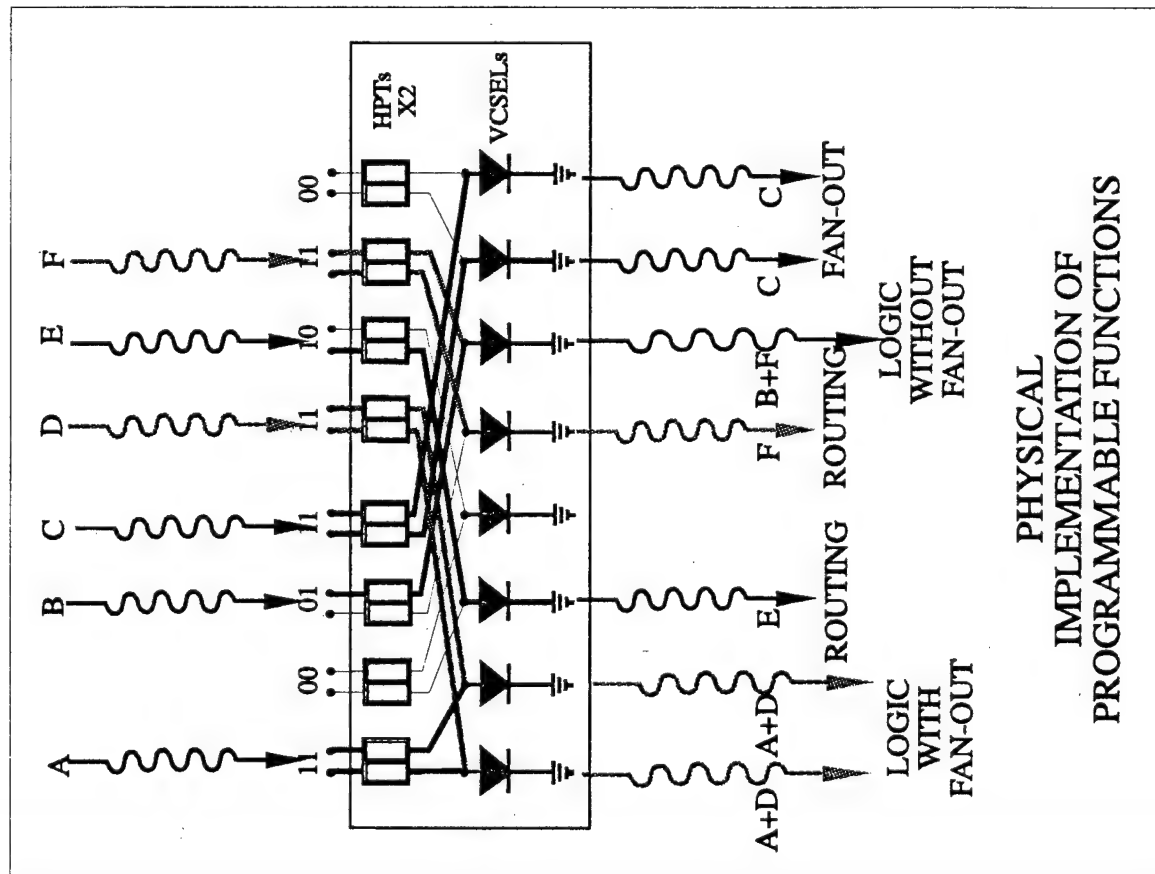
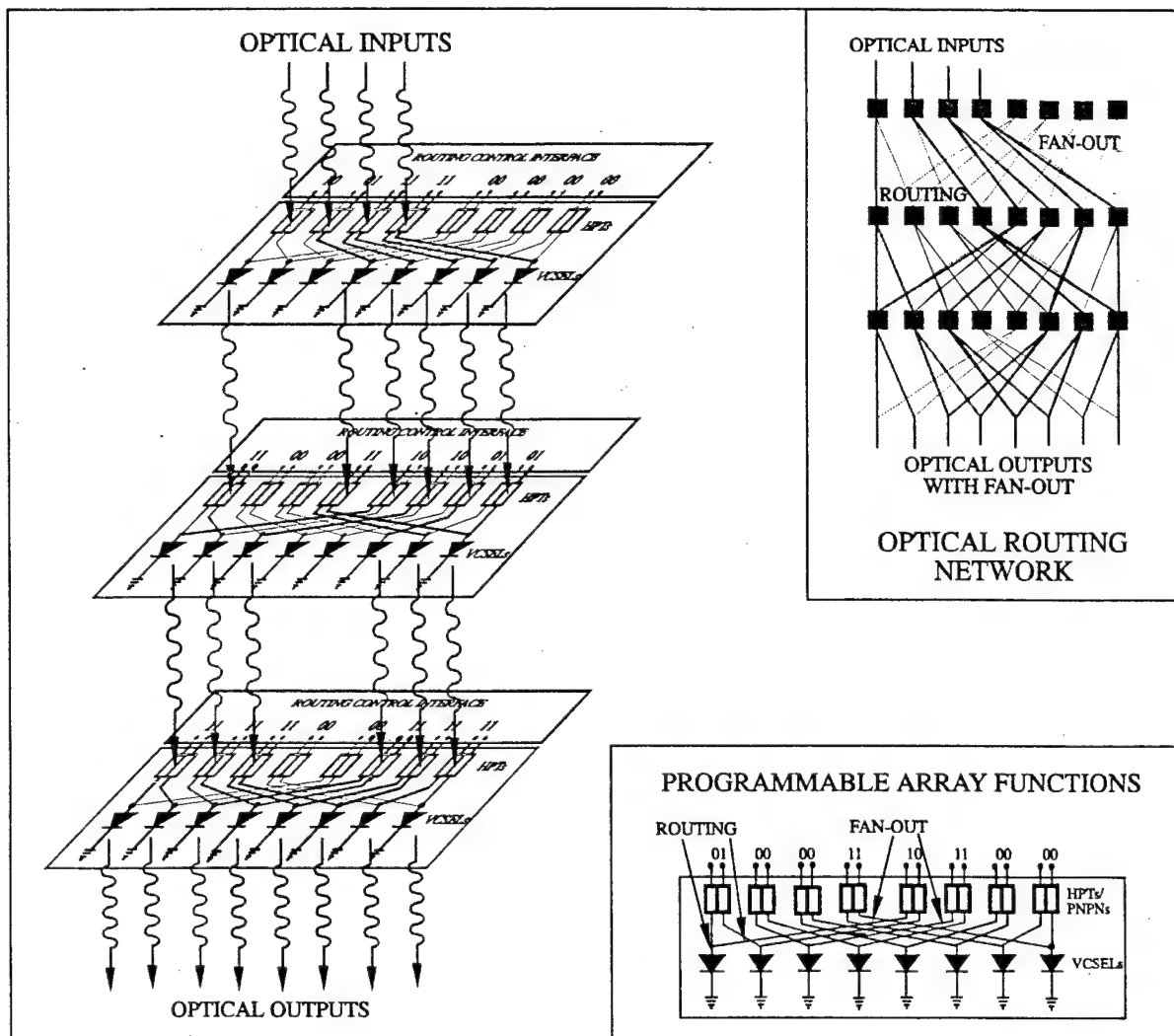


FIGURE 10.



RECONFIGURABLE 1x8 SWITCH ARRAY

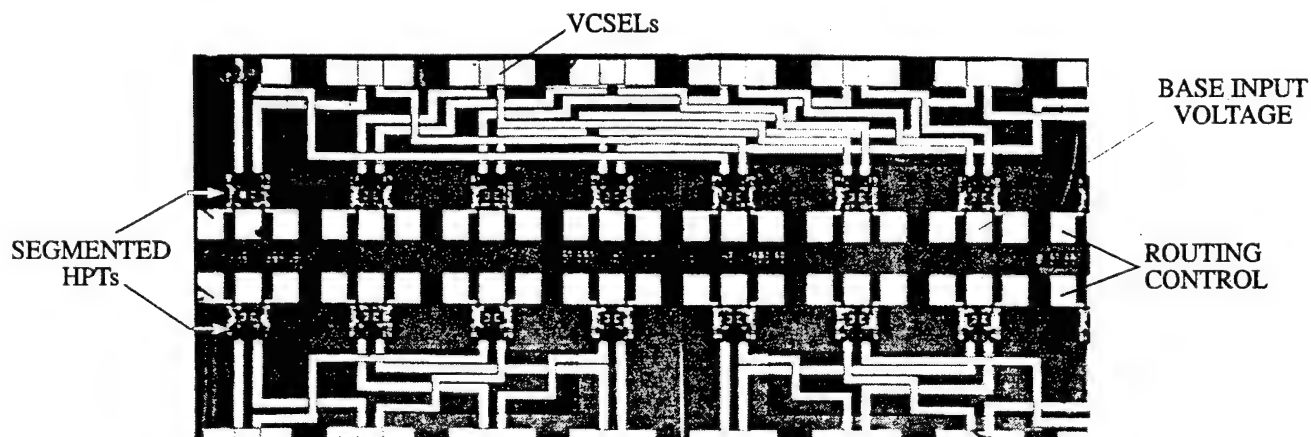


FIGURE 11.

OPTICAL BYPASS & EXCHANGE SWITCHING OPERATION

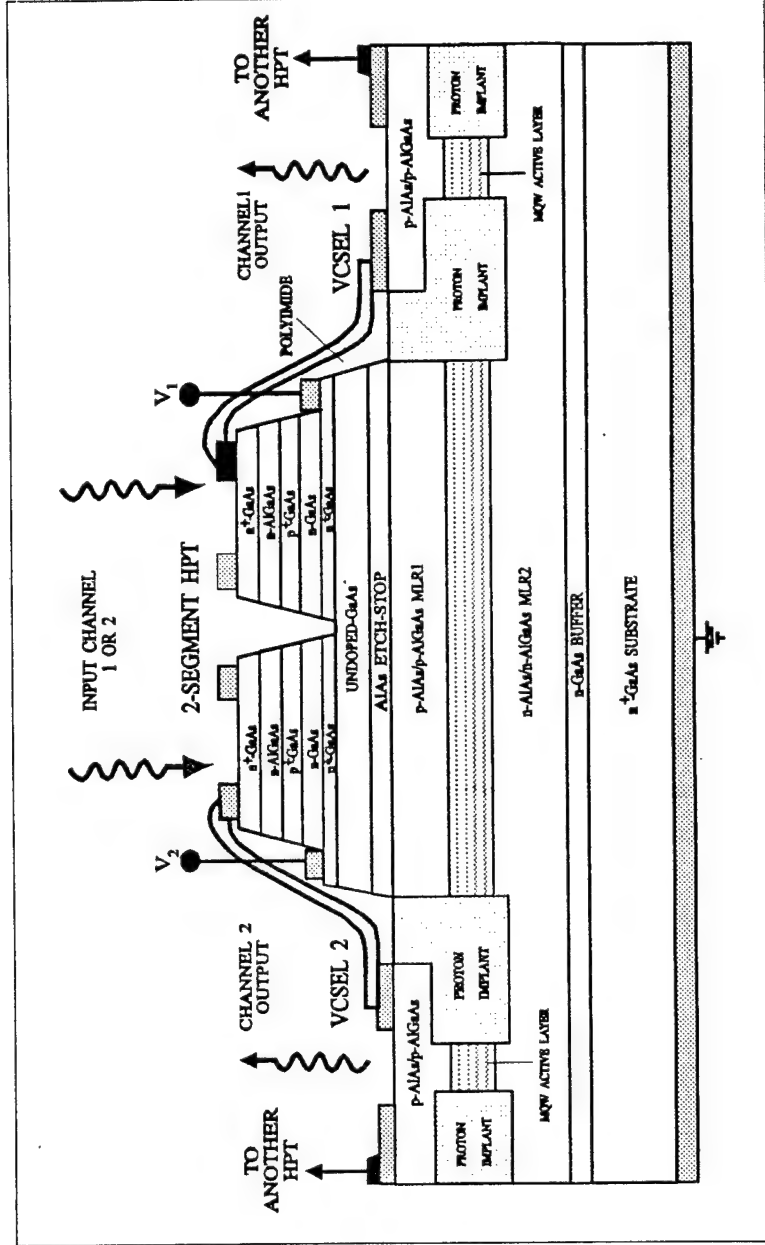
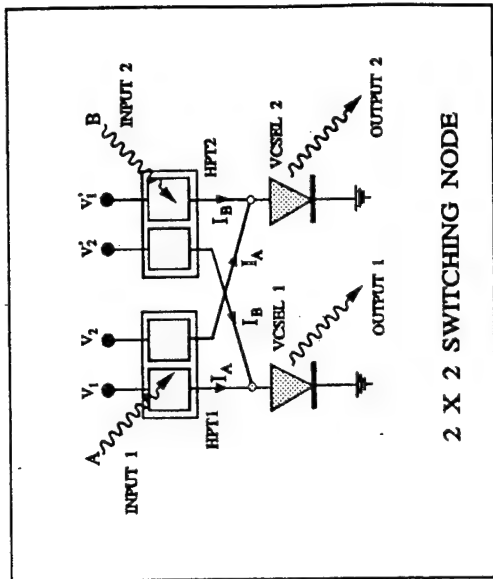
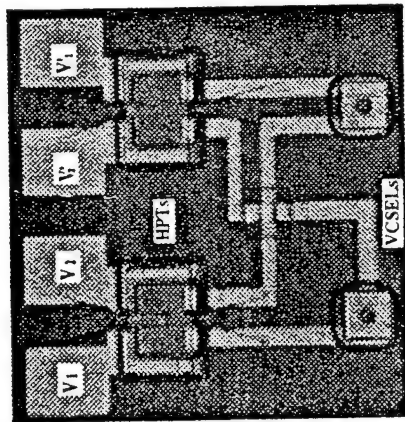
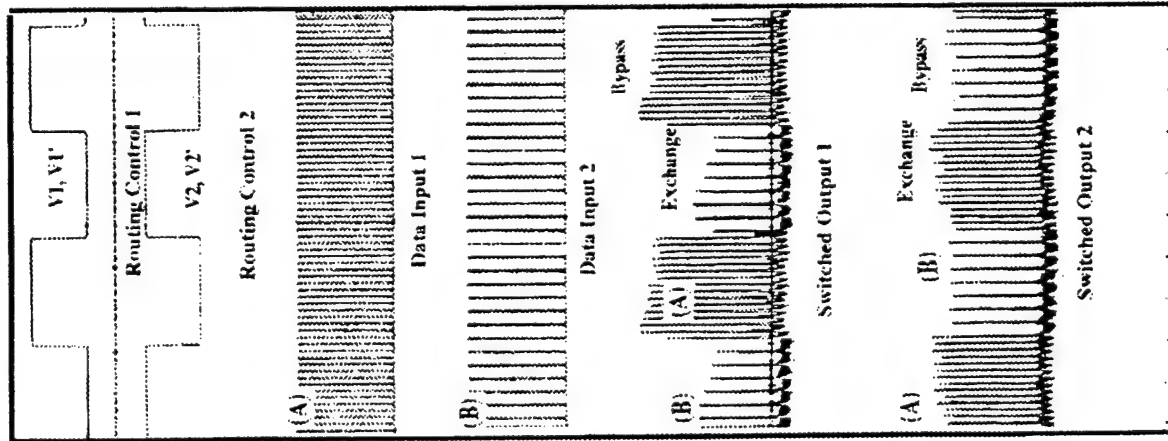
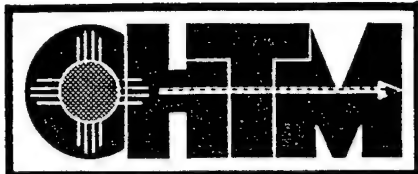
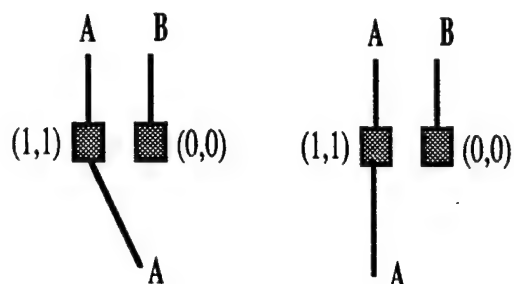


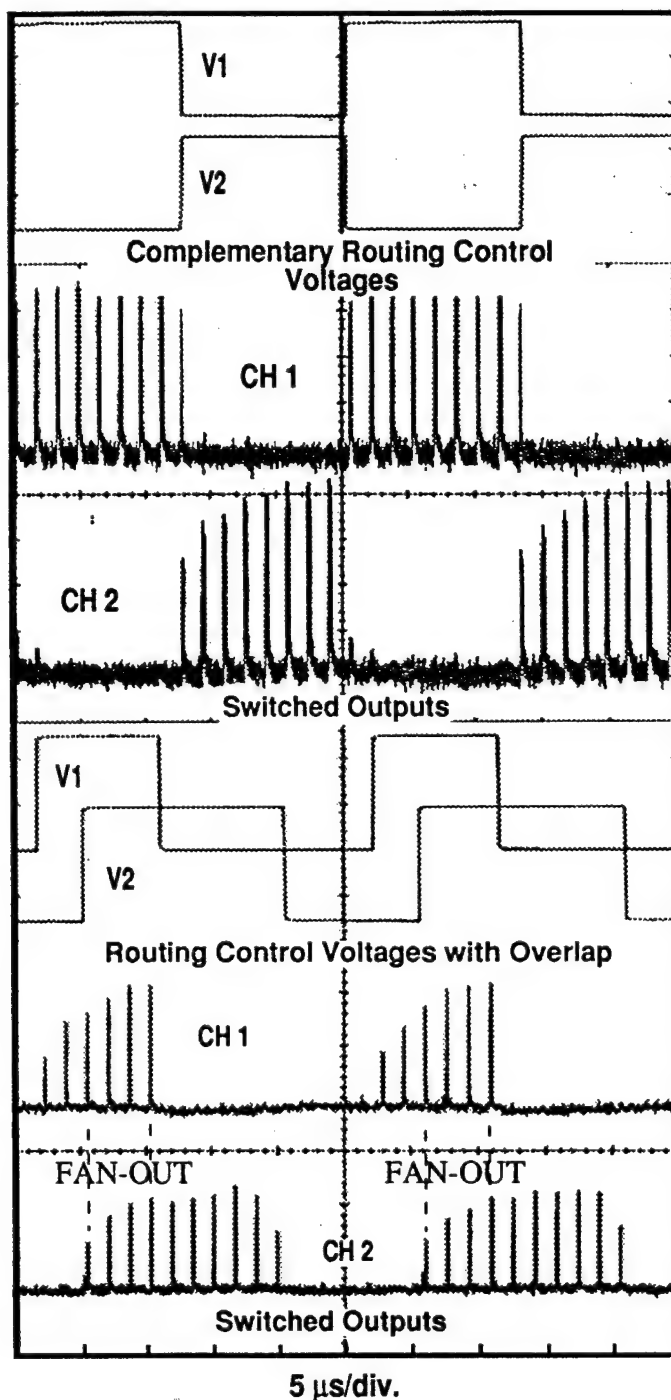
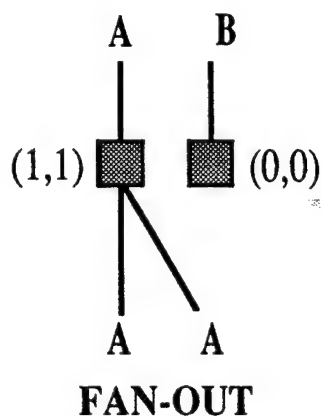
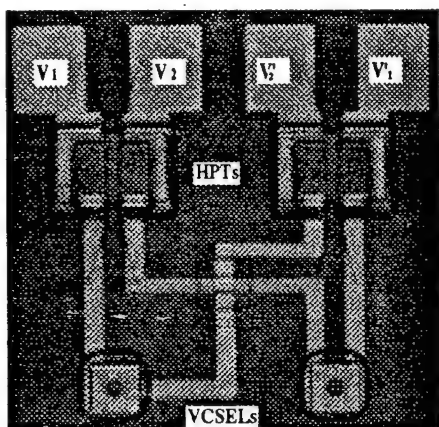
FIGURE 12a.



JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS



ROUTING



SPATIAL ROUTING OPERATIONS OF A 1X2 HPT/VCSEL OPTICAL SWITCH
WITH A FAN-OUT CAPABILITY

JULIAN CHENG

200 Mb/s ELECTRICAL AND OPTICAL MODULATION RESPONSE
OF A MONOLITHIC HPT/VCSEL SWITCH

Y.C. Lu, J. Cheng, et al.,
Electronics Letters, Vol. 31, No. 7
pp. 579-580, March 1995

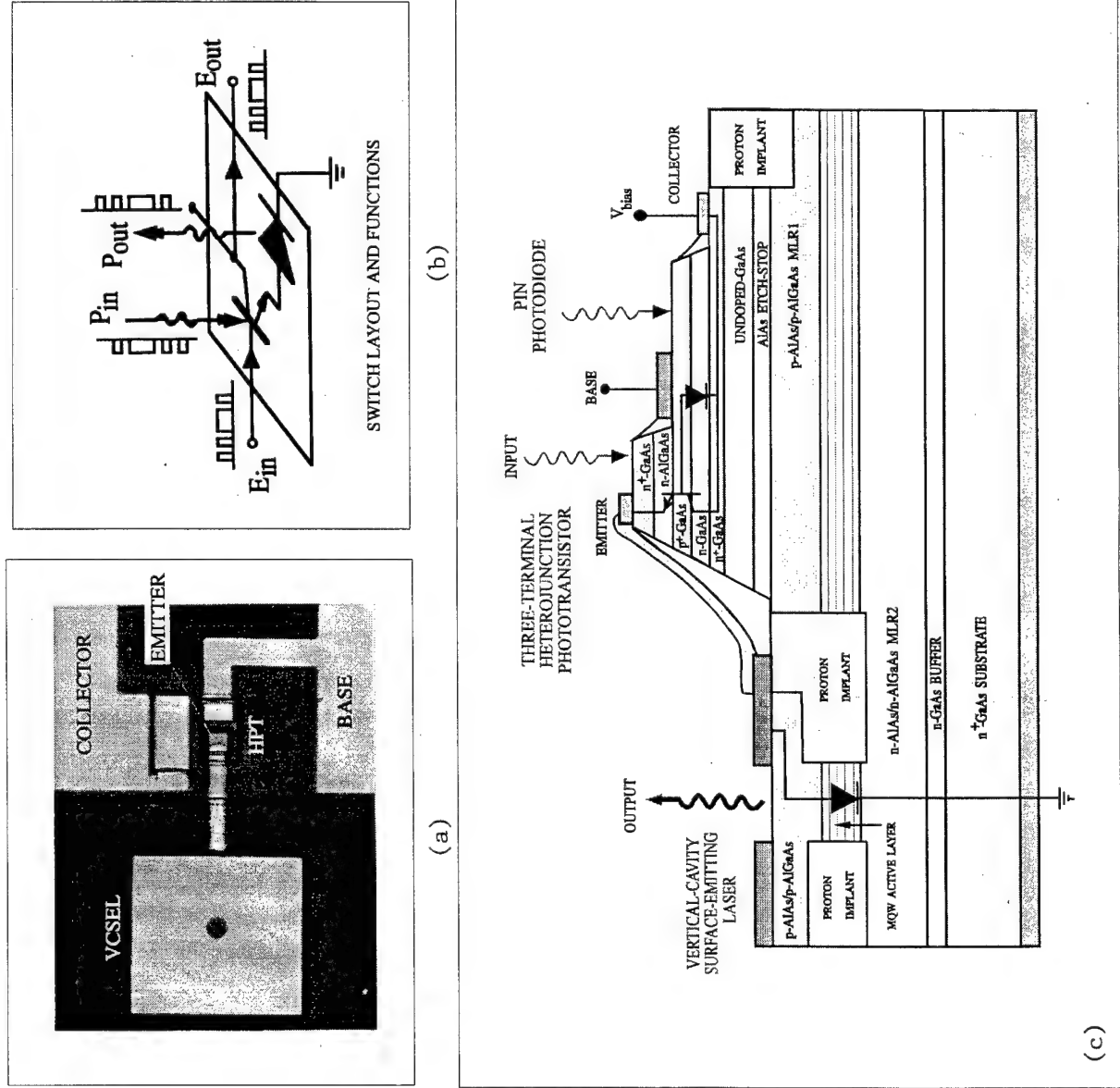
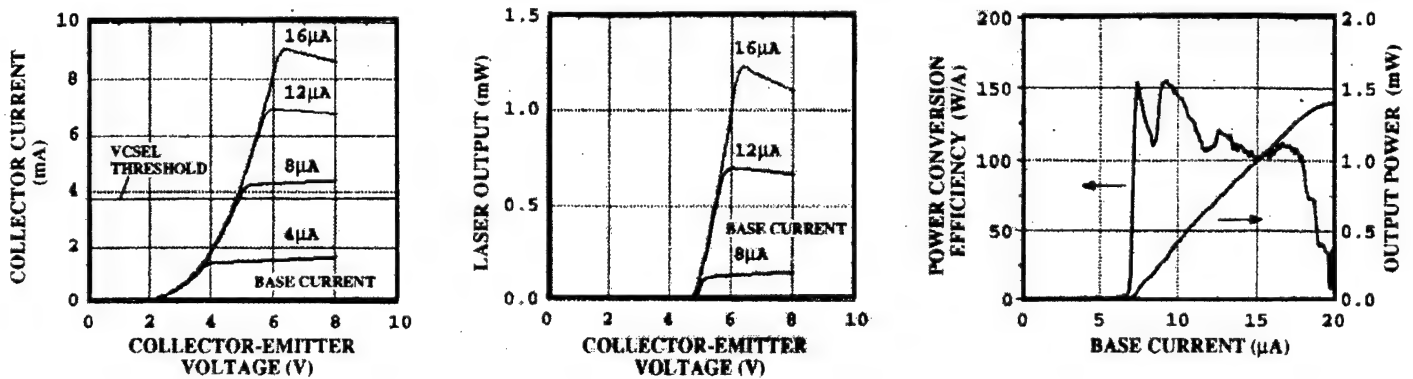


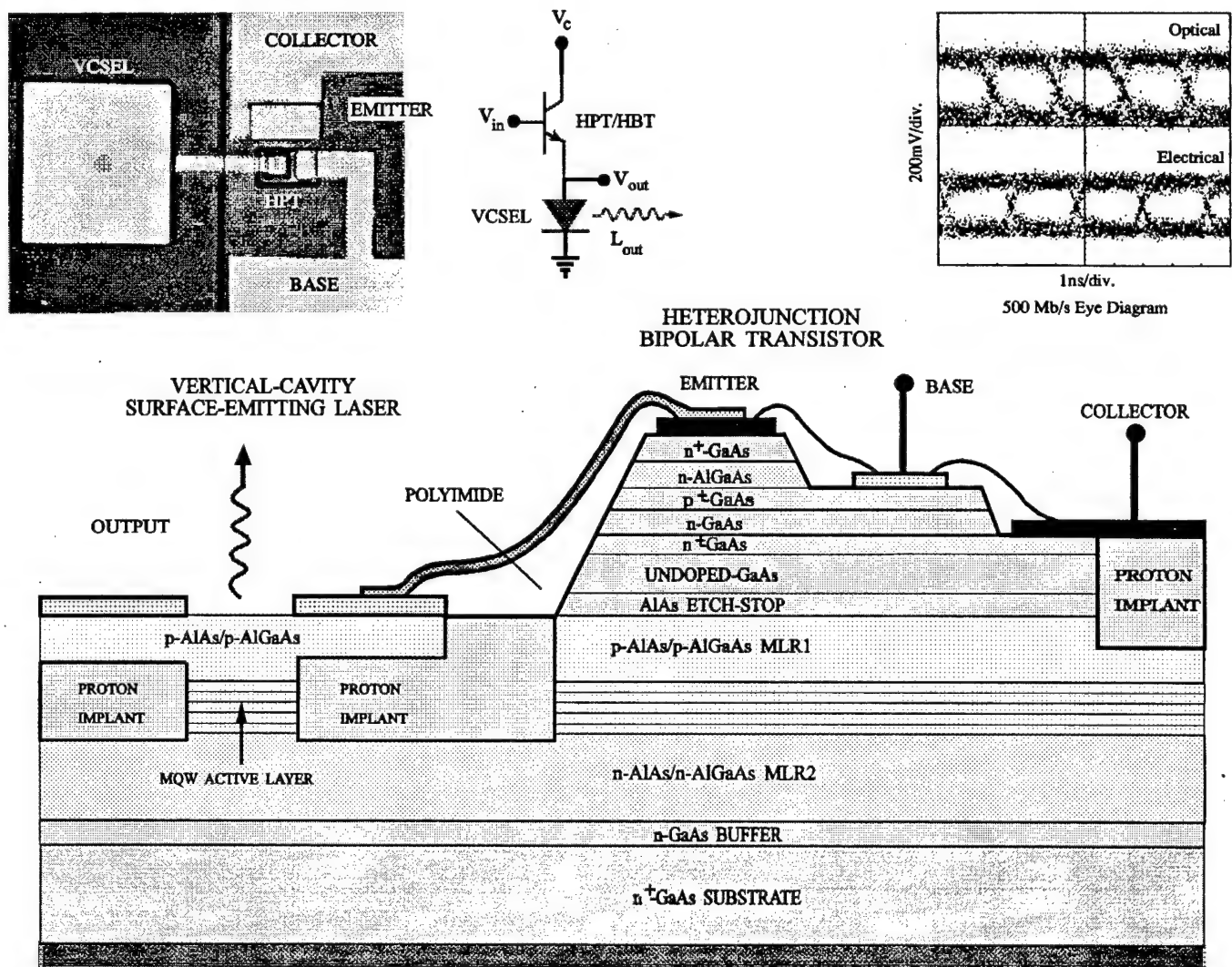
FIGURE 13.

MONOLITHIC INTEGRATION OF VERTICAL-CAVITY SURFACE-EMITTING LASER AND HETEROJUNCTION BIPOLAR TRANSISTOR

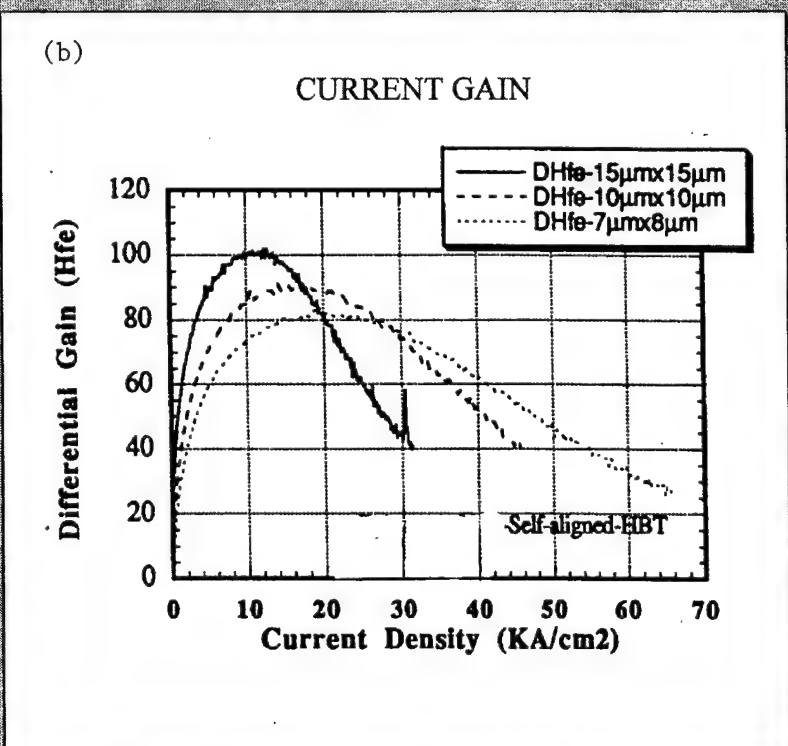
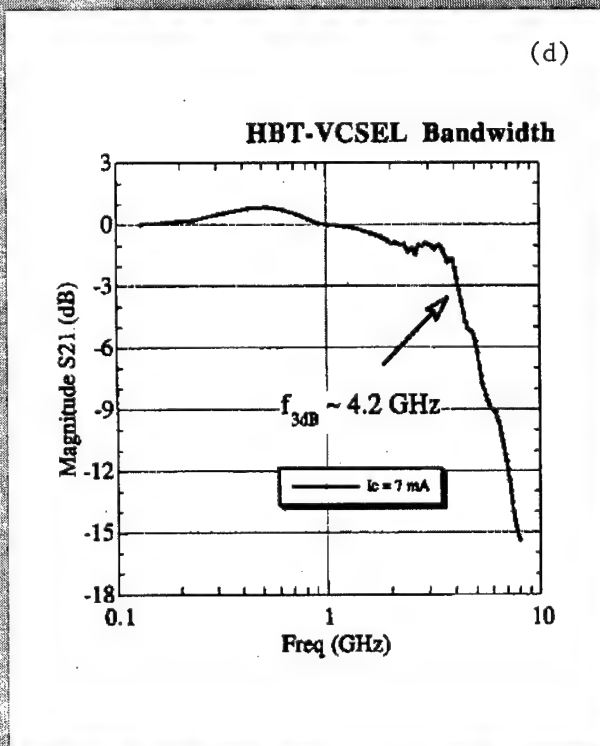
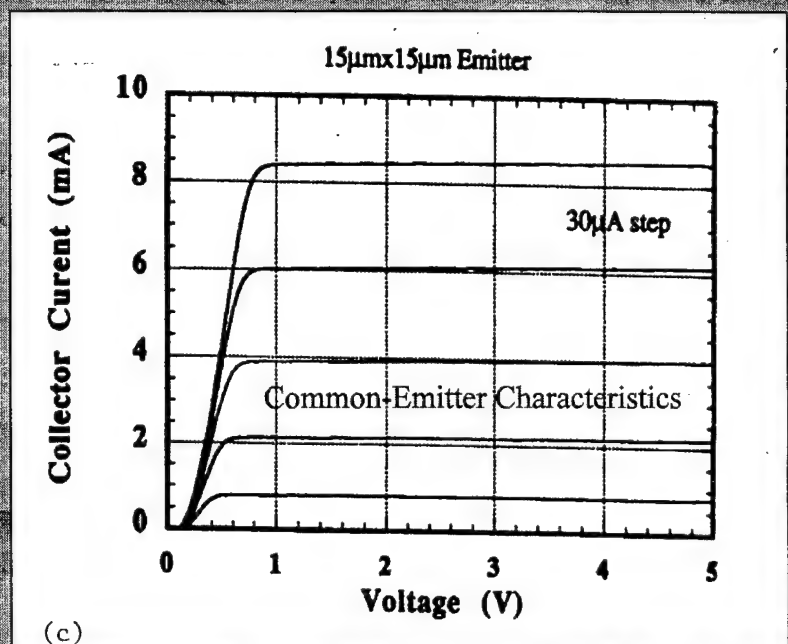
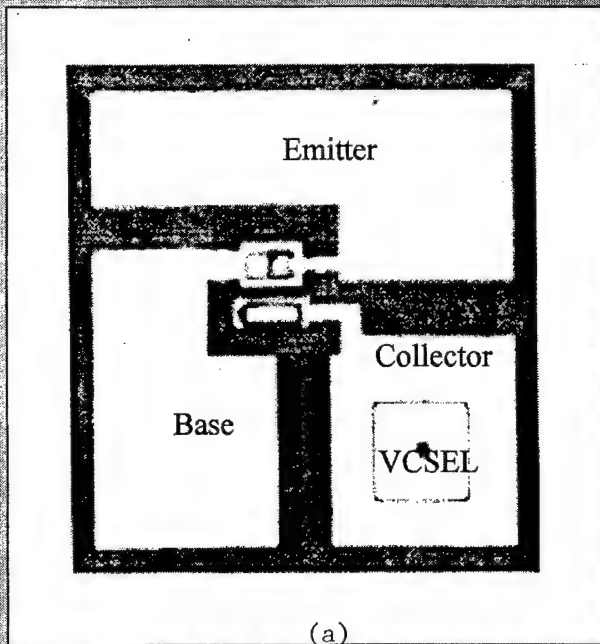
(b)



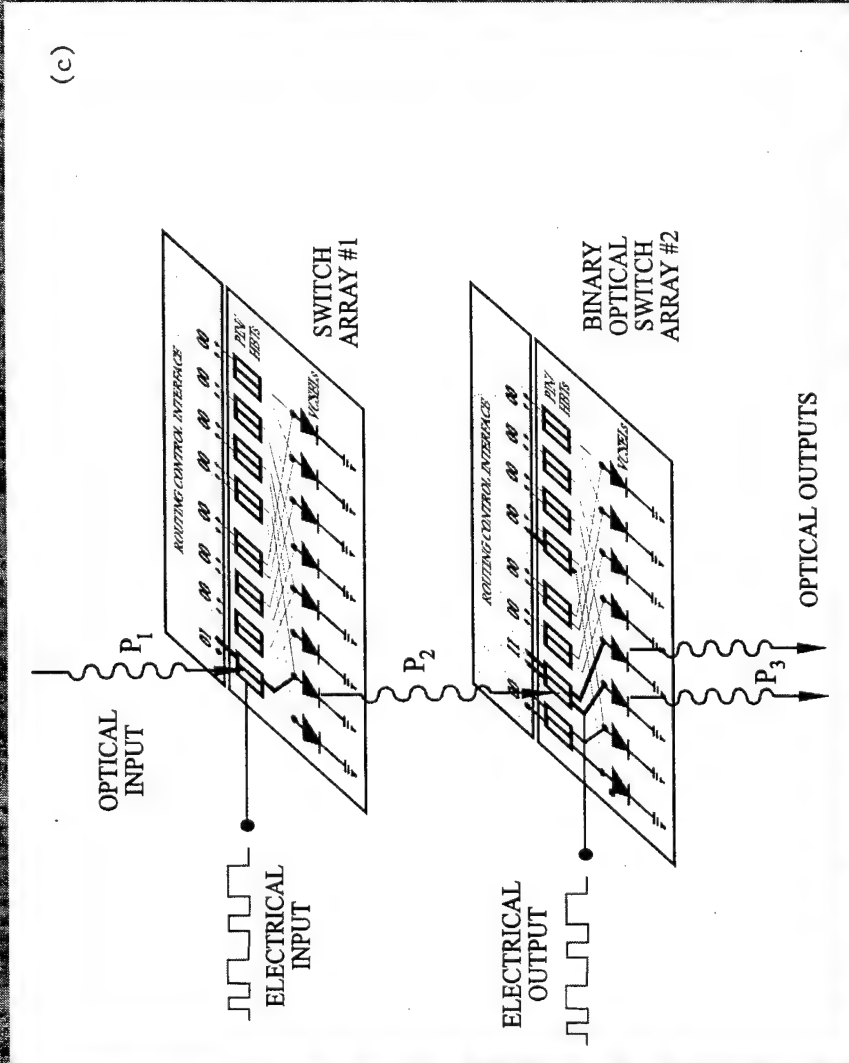
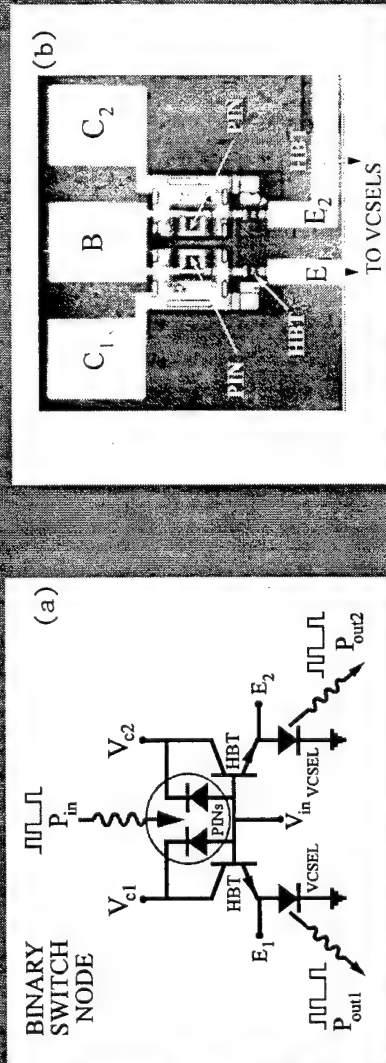
(a)



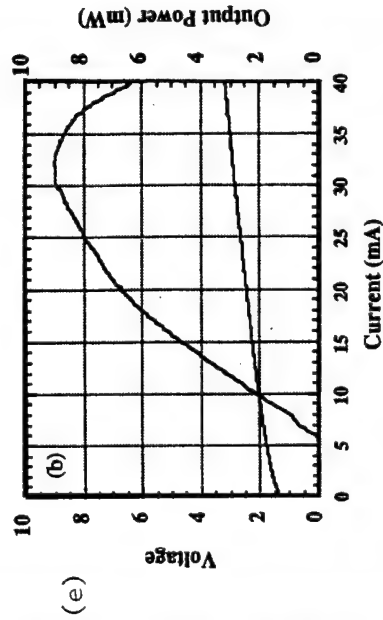
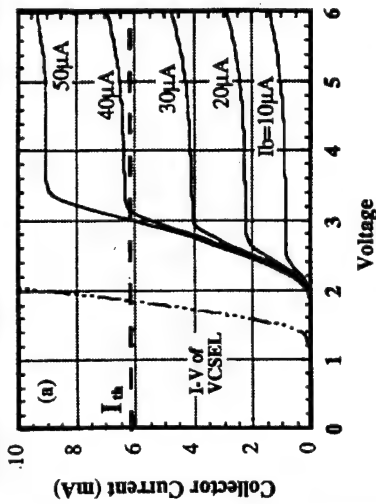
HETEROJUNCTION BIPOLAR TRANSISTOR CHARACTERISTICS IN A MONOLITHIC HBT/VCSEL SWITCH



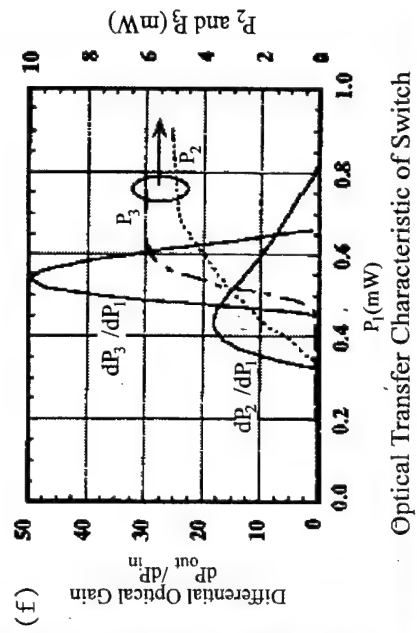
CASCADED MULTI-STAGE BINARY OPTICAL SWITCH ARRAYS



(d) Common-emitter HBT/VCSEL Characteristics



(f) Lasing & Electrical Characteristics of VCSEL



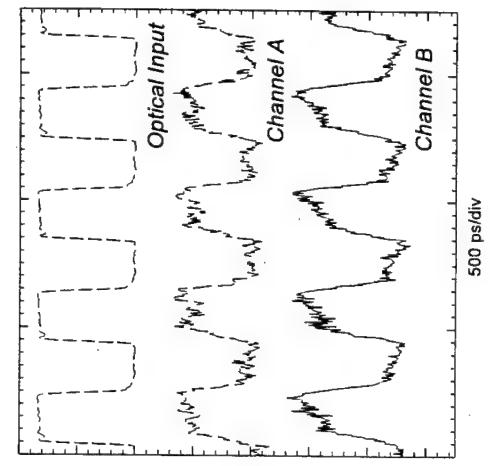
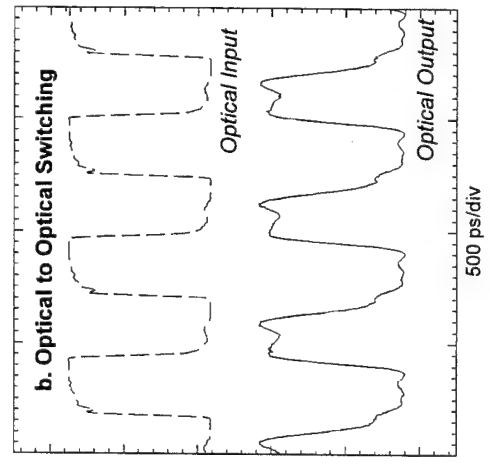
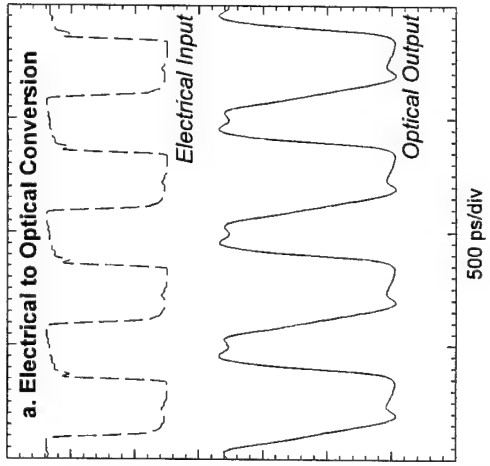
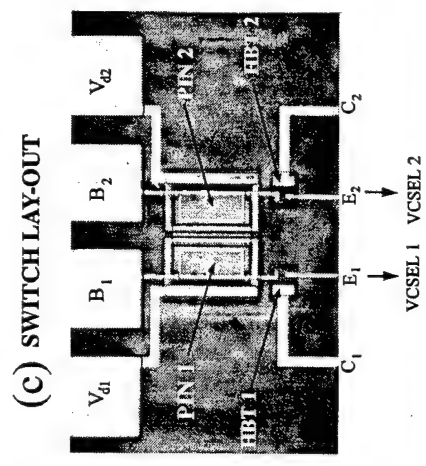
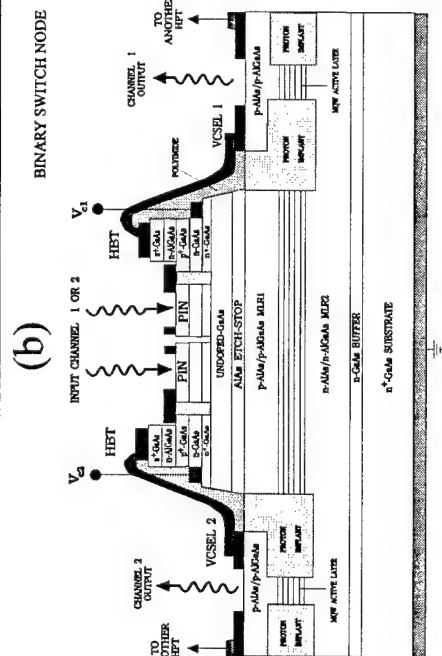
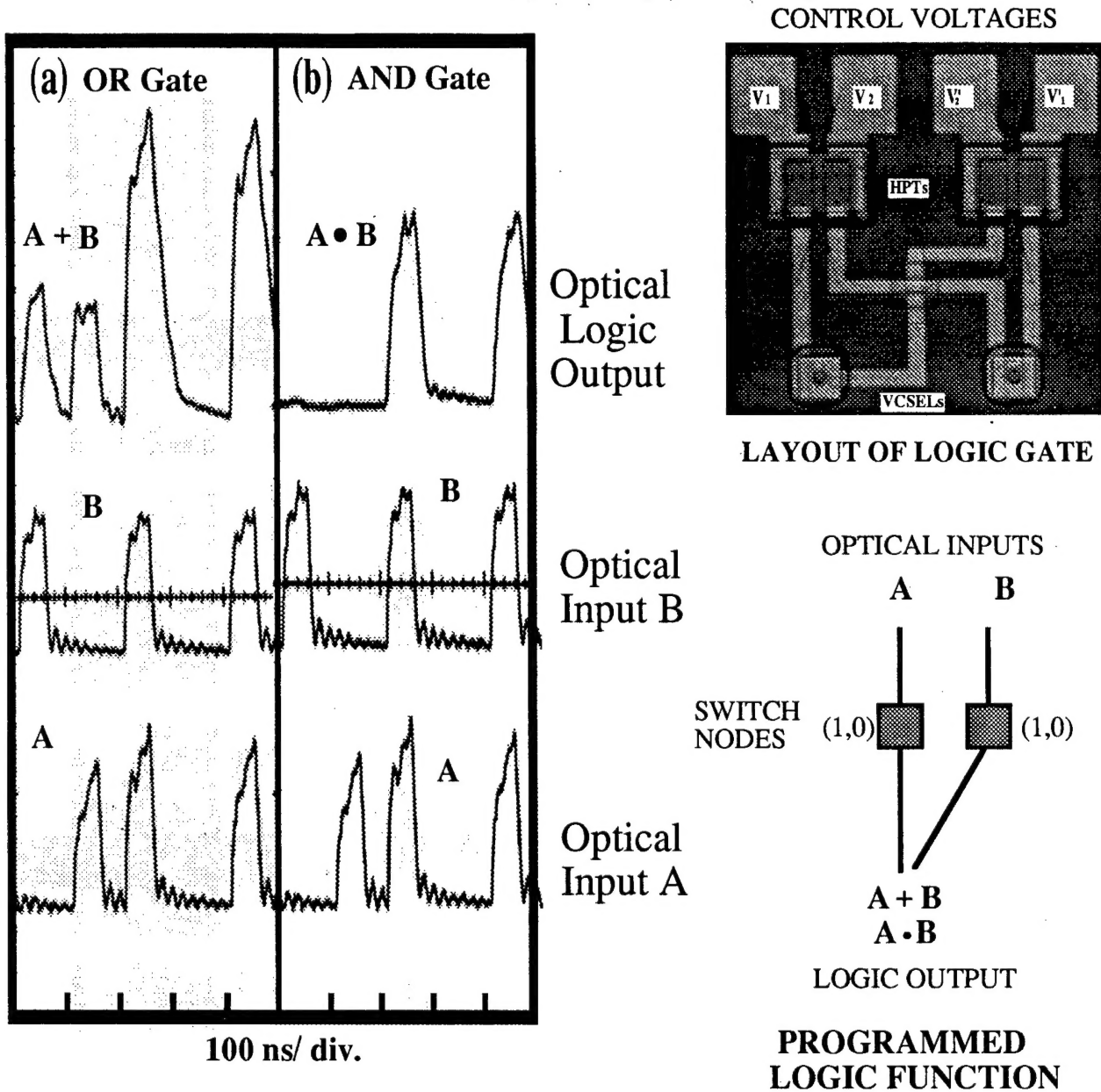


FIGURE 17.

JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS



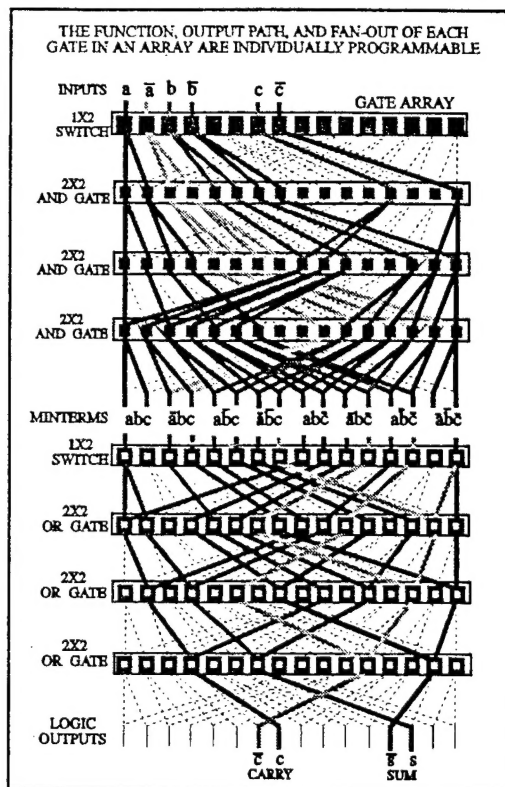
**PROGRAMMABLE OPTICAL LOGIC
 FUNCTIONS (AND & OR) WITHOUT FAN-OUT
 USING A MONOLITHIC BINARY HPT/VCSEL
 OPTICAL LOGIC GATE**

FIGURE 18.

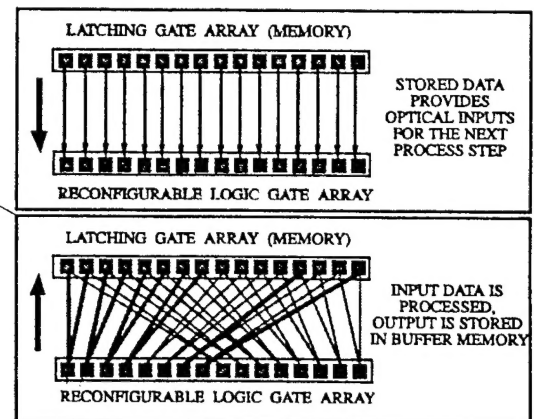


JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

CASCADED MULTI-STAGE
PROGRAMMABLE LOGIC GATE ARRAY



PROGRAMMABILITY
OF THE LOGIC ARRAY
ALLOWS THE ENTIRE
MULTI-STAGE
PROCESS SEQUENCE
TO BE FOLDED INTO A
TWO-CHIP PLGA



OPTICALLY-FOLDED TWO-CHIP
PROGRAMMABLE LOGIC GATE ARRAY

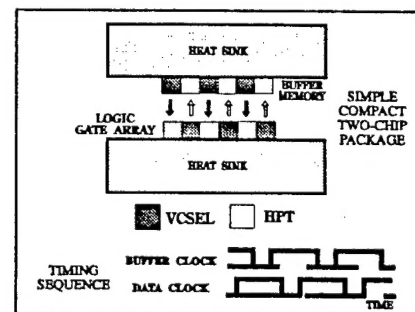
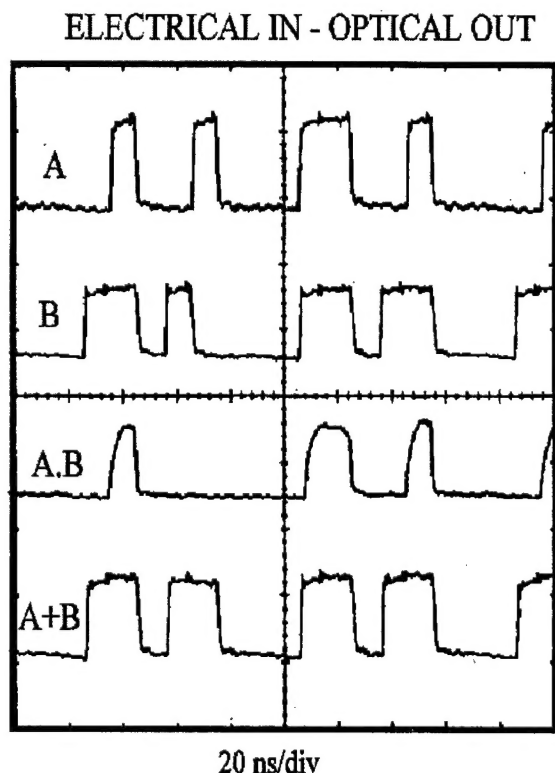
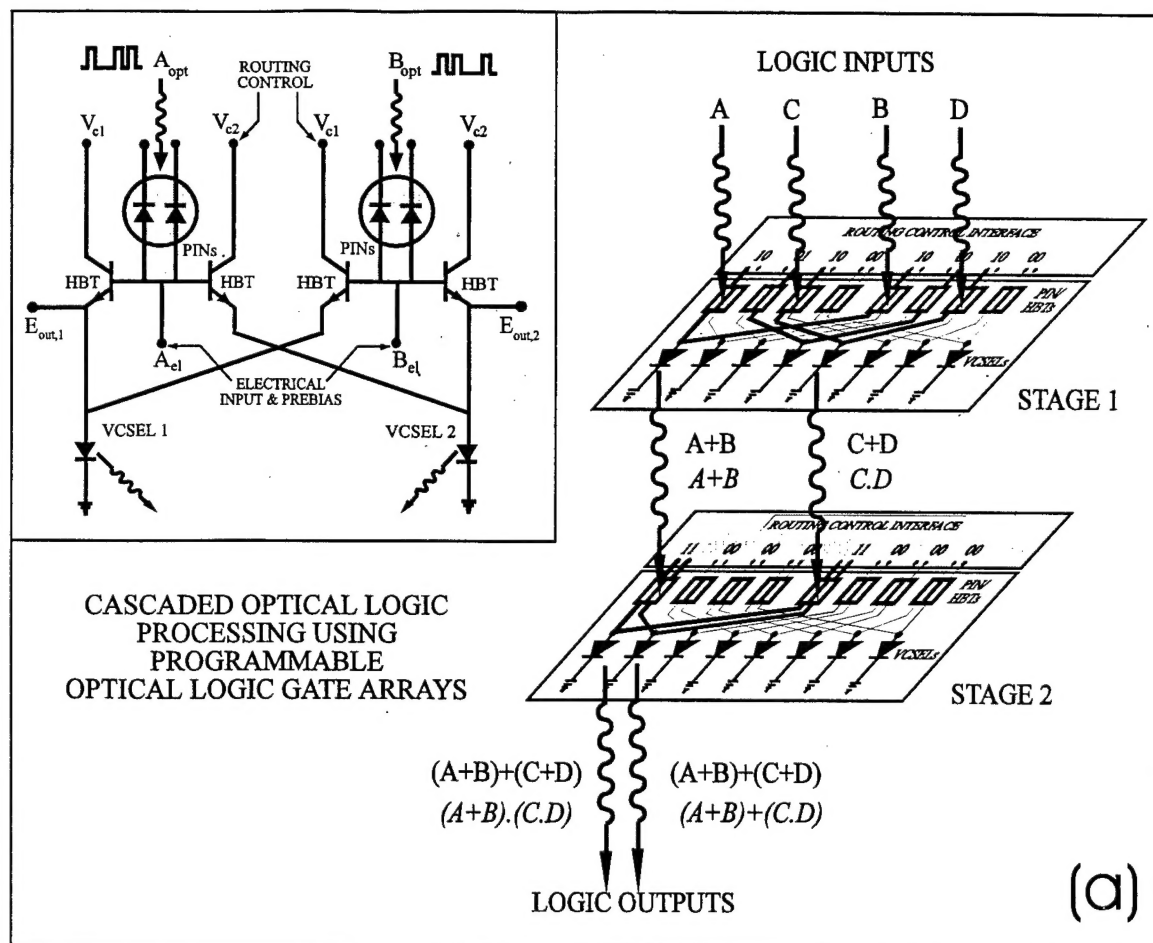
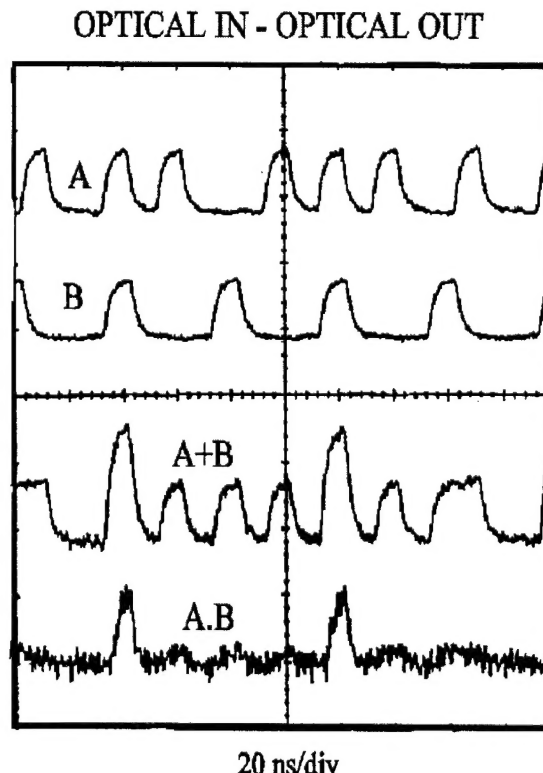


FIGURE 19.

JULIAN CHENG
University of New Mexico, Center for High Technology Materials



(b) ELECTRICAL LOGIC INPUTS
OPTICAL LOGIC OUTPUT



(c) OPTICAL LOGIC INPUTS
OPTICAL LOGIC OUTPUT

JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

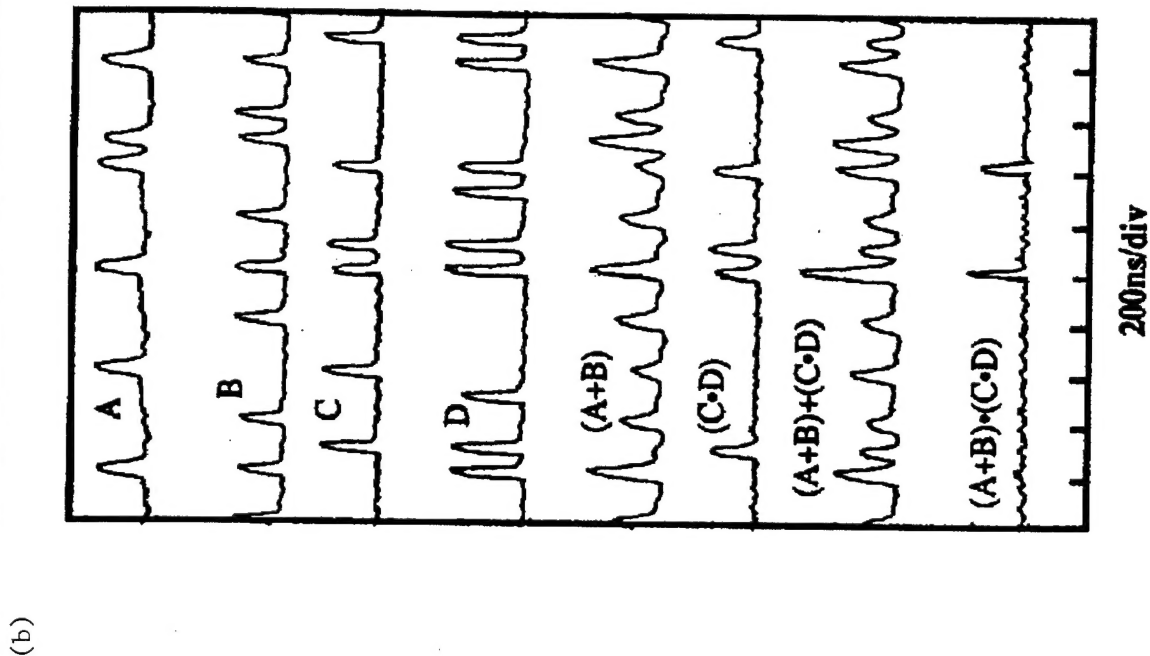
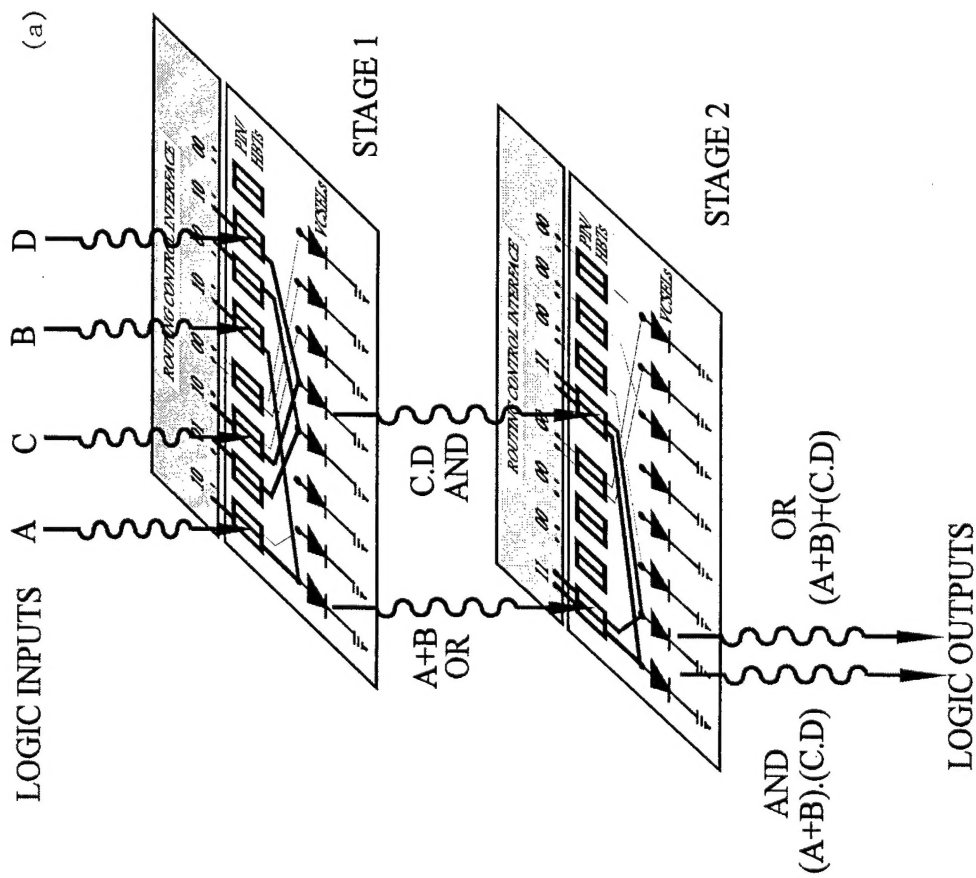


FIGURE 21.